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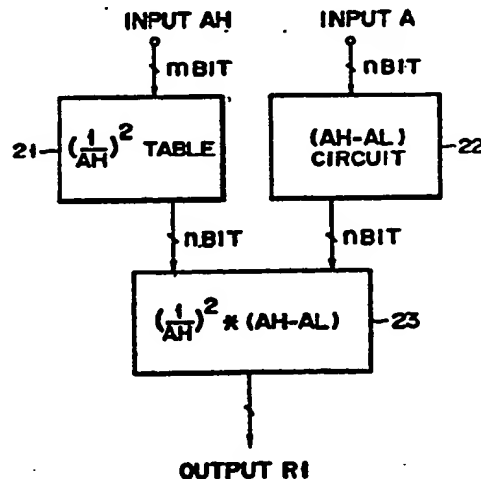
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## (54) Reciprocal arithmetic circuit with ROM table.

(57) A reciprocal arithmetic circuit for deriving the reciprocal of a divisor A includes a ROM table (21) for converting upper-bit data AH supplied as an address to the approximation of the reciprocal  $1/AH^2$  of the square thereof and outputting the same, a subtractor circuit (22) for deriving a difference (AH-AL) between the upper-bit data AH and the lower-bit data AL of the divisor A, and a multiplier circuit (23) for receiving an output ( $1/AH^2$ ) of the ROM table (21) and an output (AH-AL) of the subtractor circuit and deriving the product  $1/AH^2 \cdot (AH-AL)$  thereof to make the output ( $1/AH^2$ ) of the ROM table more nearly equal to the reciprocal  $1/A$  of the divisor A.



**FIG. 4**

## Reciprocal arithmetic circuit with ROM table

This invention relates to a reciprocal arithmetic circuit for deriving a reciprocal  $1/A$  of a divisor  $A$ , and more particularly to a reciprocal arithmetic circuit used in a divider circuit.

In general, a division  $B/A$  is calculated by multiplying the reciprocal  $1/A$  of a divisor  $A$  by a dividend  $B$ . A typical example of a divider circuit of performing the division  $B/A$  is shown in Fig. 1. In Fig. 1, 1 denotes a conversion table for converting the divisor  $A$  into the reciprocal  $1/A$  and the conversion table is constituted by a read only memory (ROM). In Fig. 1, 2 denotes a multiplier circuit.

All the bits of the divisor  $A$  are supplied as an address signal to the conversion table 1 and reciprocal table information stored in the conversion table 1 is searched for according to the address signal. However, in the all-bit or full-bit method in which all the bits of the divisor  $A$  are used, it is necessary for the ROM constituting the conversion table to have an extremely large memory capacity. For example, when the divisor  $A$  is of 16 bits and the reciprocal  $1/A$  is expressed by 16 bits, the memory capacity of the ROM must be  $2^{16}$  words or  $2^{16} \times 16 = 1$  Mbits. In this way, in the full-bit method in which the reciprocal  $1/A$  is derived by use of all the bits of the divisor  $A$ , a large ROM memory capacity is necessary, increasing the cost of a LSI in which the divider circuit is integrated.

In general, an approximation arithmetic method using Newton's method is used as an arithmetic method of deriving the reciprocal  $1/A$  with a small ROM memory capacity.

In the above approximation arithmetic method, upper-digit bits  $AH$  of the divisor  $A$  are first input as an address signal to the conversion table and table information of the conversion table is searched for according to the address signal. As a result, the primary approximate reciprocal  $1/AH$  of the divisor  $A$  can be derived. Next, the primary approximate reciprocal  $1/AH$  is subjected to the approximation process of Newton's method to derive the secondary approximate reciprocal which is more precise than the primary approximate reciprocal.

Now, the approximate calculation according to Newton's method is explained. Fig. 2 is a flowchart showing the approximate calculation according to Newton's method.

First, upper  $m$ -bit data  $AH$  of the divisor  $A$  are used as an address signal to search for table information in the ROM, thus deriving the primary approximate reciprocal  $R0 = 1/AH$  (steps S1 to S3). Then, the secondary approximate reciprocal  $R1$  is derived by use of the following approximate equation (steps S4 and S5):

$$R1 = R0 \cdot (2 - A \cdot R0) \quad (1)$$

Further,  $R1$  is used instead of  $R0$  in Eq. (1) to calculate the same. As the calculation process is repeatedly effected, the secondary approximate reciprocal  $R1$  more approaches to the reciprocal  $1/A$  of  $A$ . A counter  $C$  counts the number of calculations, and the calculation of Eq. (1) is repeatedly effected until the count of the counter  $C$  reaches a preset loop number  $N$ . Therefore, the secondary approximate reciprocal  $R1$  becomes more nearly equal to the reciprocal  $1/A$  of the divisor  $A$  as the loop number  $N$  becomes larger.

Fig. 3 shows the relation between the bit number  $m$  of the upper-bit data  $AH$ , the size of the ROM constituting the conversion table and the loop number  $N$  in a case where the full-bit number of the divisor  $A$  is set to 16 bits.

As is clearly understood from Fig. 3, the ROM size becomes smaller as the bit number  $m$  of the upper-bit data  $AH$  becomes smaller. In contrast, an error in the primary approximate reciprocal  $R0$  becomes larger as the bit number  $m$  of the upper-bit data  $AH$  becomes smaller, thereby making it necessary to increase the loop number  $N$ .

The approximate equation by Newton's method shown in Eq. (1) includes two multiplications. Therefore, in the approximate equation by Newton's method, it is necessary to effect multiplications of a number twice the loop number  $N$ . Since the multiplication is effected by repeatedly effecting additions, it takes a long time to effect the multiplication. Therefore, in the Newton's method, there occurs a problem that the loop number  $N$  becomes larger if the ROM size is reduced, and as a result time required for effecting the approximate calculation becomes larger.

An object of this invention is to provide a reciprocal arithmetic circuit in which a high-speed and highly precise reciprocal calculation can be effected and the hardware construction can be made simple.

According to this invention, there is provided a reciprocal arithmetic circuit comprising conversion table means storing approximate information items corresponding to the reciprocals  $[(1/AH)^2]$  of the square of upper-bit data  $AH$  of divisors  $A$ , for converting the upper-bit data  $AH$  supplied as an address into the approximation of the squared reciprocal  $[(1/AH)^2]$  and outputting the approximation; subtract means for deriving a difference  $(AH-AL)$  between the upper-bit data  $AH$  and lower-bit data  $AL$  of the divisor  $A$ ; and multiplier means connected to receive an output  $[(1/AH)^2]$  of the conversion table means and an output  $(AH-$

AL) of the subtracter means, for deriving the product  $[(1/AH)^2 \cdot (AH-L)]$  thereof to make the output  $[(1/AH)^2]$  of the conversion table means more nearly equal to the reciprocal  $1/A$  of the divisor A.

In the reciprocal arithmetic circuit, a precalculation or the subtraction  $(AH-AL)$  is effected by the subtracter means using the lower-bit data AL prior to the calculation by multiplier means. Therefore, the approximate calculation for approximating the output  $[(1/AH)^2]$  of the conversion table means to the reciprocal  $1/A$  of the divisor A can be effected by a simple operation of multiplying the output  $[(1/AH)^2]$  of the conversion table means by the output  $(AH-AL)$  of the subtracter means. Further, since the subtraction  $(AH-AL)$  by the subtracter means is effected while the conversion operation is being effected by the conversion table, the operation time is not increased because of the subtracting operation of the subtracter means. In this way, according to the reciprocal arithmetic circuit, the precalculation is effected by use of the lower-bit data AL prior to the approximate calculation and the high-speed reciprocal calculation can be effected by the simple hardware.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing the construction of an ordinary divider circuit;

Fig. 2 is a flowchart for illustrating the approximate calculation method by using Newton's method;

Fig. 3 is a diagram showing the relation between the ROM size and the number of calculations in a case where the approximate calculation method shown in Fig. 2 is effected;

Fig. 4 is a block diagram showing a reciprocal arithmetic circuit according to a first embodiment of this invention;

Fig. 5 is a flowchart showing the operation of the reciprocal arithmetic circuit shown in Fig. 4;

Figs. 6A to 7B are diagrams showing the characteristics of the approximate calculation effected by the reciprocal arithmetic circuit shown in Fig. 4;

Fig. 8 is a block diagram showing a reciprocal arithmetic circuit according to a second embodiment of this invention;

Fig. 9 is a flowchart showing the operation of the reciprocal arithmetic circuit shown in Fig. 8;

Fig. 10 is a block diagram showing a reciprocal arithmetic circuit according to a third embodiment of this invention;

Fig. 11 is a flowchart showing the operation of the reciprocal arithmetic circuit shown in Fig. 10;

Figs. 12A to 13B are diagrams showing the characteristics of the approximate calculation effected by the reciprocal arithmetic circuit according to the second embodiment of this invention shown in Fig. 8;

Fig. 14 is a block diagram showing a reciprocal arithmetic circuit according to a fourth embodiment of this invention;

Fig. 15 is a block diagram showing the detail construction obtained by applying the principle of a correction process by the reciprocal arithmetic circuit according to the fourth embodiment of this invention to the reciprocal arithmetic circuit of Fig. 4 according to the first embodiment;

Fig. 16 is a flowchart showing the correction process by the reciprocal arithmetic circuit shown in Fig. 15;

Figs. 17A to 18C are diagrams showing the characteristics of the correction process effected by the reciprocal arithmetic circuit shown in Fig. 15;

Fig. 19 is a block diagram showing a reciprocal arithmetic circuit according to a fifth embodiment of this invention;

Fig. 20 is a flowchart showing the operation of the reciprocal arithmetic circuit shown in Fig. 19;

Fig. 21 is a diagram showing the relation between the number of bits of the divisor A and the ROM size in the reciprocal arithmetic circuit shown in Fig. 19;

Fig. 22 is a block diagram showing a reciprocal arithmetic circuit according to a sixth embodiment of this invention;

Fig. 23 is a flowchart showing the operation of the reciprocal arithmetic circuit shown in Fig. 22; and

Fig. 24 is a diagram showing the relation between the number of bits of the divisor A and the ROM size in the reciprocal arithmetic circuit shown in Fig. 22.

Fig. 4 shows a reciprocal arithmetic circuit according to a first embodiment of this invention. The reciprocal arithmetic circuit derives an approximation of the reciprocal  $1/A$  of the divisor A. First, the principle of the approximate calculation for deriving the approximation is explained.

In order to obtain the approximation of the reciprocal of the divisor A, the divisor A is first divided into upper m-bit data AH and lower (n-m)-bit data AL. That is, the divisor A can be expressed by the following equation:

$$A = AH + AL \quad (2)$$

Assume that A is expressed as follows:

$$A = a_1 \cdot (1/2) + a_2 \cdot (1/2)^2 + \dots + a_n \cdot (1/2)^n \quad (3)$$

Then, the following equations can be obtained:

$$AH = a_1 \cdot (1/2) + a_2 \cdot (1/2)^2 + \dots + a_m \cdot (1/2)^m \quad (4)$$

$$AL = a_{m+1} \cdot (1/2)^{m+1} + \dots + a_n \cdot (1/2)^n \quad (5)$$

The approximation is derived as follows:

First, the approximation R1 of the reciprocal  $1/A$  can be expressed by the following equation:

$$R1 = \frac{1}{A} = \frac{1}{AH+AL} = \frac{AH-AL}{AH^2-AL^2} \quad \text{--- (6)}$$

In this case, assume the following condition:  $AH^2 \gg AL^2$  (7)

Then, the following approximation can be obtained:  $R1 \approx \left(\frac{1}{AH}\right)^2 \cdot (AH-AL)$  (8)

Thus, the reciprocal arithmetic circuit of the first embodiment effects the approximate calculation expressed by Eq. (8).

A ROM table 21 of Fig. 4 stores approximation information corresponding to the square reciprocals  $[(1/AH)^2]$  of the upper-bit data AH of divisors A. The ROM table 21 receives the upper m-bit data AH of the divisor A as an address signal, converts the data AH into the reciprocal  $[(1/AH)^2]$  of the square of the data AH and outputs the converted value. The output  $[(1/AH)^2]$  consists of n bits. A subtractor circuit 22 derives a difference (AH-AL) between the upper m-bit data AH and lower (n-m)-bit data AL. An output (AH-AL) of the subtractor circuit 22 consists of n bits. The output  $[(1/AH)^2]$  of the ROM table 21 and the output (AH-AL) of the subtractor circuit 22 are respectively supplied to first and second input terminals of a multiplier circuit 23. The multiplier circuit 23 multiplies the output  $[(1/AH)^2]$  of the ROM table 21 by the output (AH-AL) of the subtractor circuit 22, and the output R1 of the multiplier circuit 23 becomes  $(1/AH)^2 \cdot (AH-AL)$ .

The result is equal to Eq. (8) and R1 determined by the approximate calculation is the approximation of the reciprocal  $1/A$ .

In the approximate calculation, the approximation R1 can be made most nearly equal to the reciprocal  $1/A$  when the bit number m of the upper-bit data AH is set to be larger than one half the bit number n of the divisor A, that is,  $m \geq n/2$ .

Fig. 5 is a flowchart showing the flow of the approximate calculation process of the reciprocal arithmetic circuit shown in Fig. 4. That is, table information is searched for according to the upper m-bit data AH of the divisor A supplied as an address signal and  $(1/AH)^2$  is detected by the searching operation (steps S21 and S22). Then,  $(1/AH)^2$  is used instead of R0 in the following equation (21).

$$R1 = R0 \cdot (AH-AL) \quad (21)$$

After this, Eq. (21) is calculated (step S24). R1 is the reciprocal approximation to be obtained in the first embodiment.

Figs. 6A and 6B show the approximate calculation characteristics of the reciprocal arithmetic circuit of Fig. 4. That is, Fig. 6A shows the relation between the divisor A and the reciprocal  $1/A$  in a case where the divisor A is increased in the step of  $(1/2)^m$ . The line L1 in Fig. 6A shows an ideal relation therebetween and the line L2 shows a relation therebetween obtained by the approximate calculation of the reciprocal arithmetic circuit of the first embodiment.

In Fig. 6B, the magnitude of the error in the reciprocal approximation obtained by the reciprocal arithmetic circuit of the first embodiment is shown.

Figs. 7A and 7B are enlarged views respectively corresponding to Figs. 6A and 6B and show the approximate calculation characteristics in one step of variation in the divisor A or in that range of the divisor A which lies between  $(1/2) + (1/2)^m$  and  $(1/2) + 2(1/2)^m$ . As is clearly seen from Fig. 7B, the magnitude of the error becomes smaller than 1 [LSB] when the lower-bit data AL satisfies that  $0 \leq AL < AL1$ , it changes from 1 to 2 [LSB] inclusive when  $AL1 \leq AL < AL2$ , and it becomes larger than 2 [LSB] when  $AL2 \leq AL$ .

Now, the reciprocal arithmetic circuit of the first embodiment is explained by comparing the reciprocal arithmetic circuit based on the Newton's method. In the approximate calculation by the Newton's method, it is necessary to effect two multiplications and one subtraction for each calculation loop as shown in Eq. (1). In contrast, the approximate calculation of the first embodiment can be effected by effecting one multiplication and one subtraction as shown by Eq. (8). Further, the subtraction in the first embodiment is previously effected prior to the multiplication while the conversion process of  $(1/AH)^2$  is being effected by use of the ROM table 21. Therefore, all the necessary calculation time required for the actual approximate calculation is not increase because of the subtracting operation.

In this way, the approximate calculation process can be simplified, the hardware for the calculation can

be made simple in construction and the operation speed of the approximate calculation process can be enhanced.

Fig. 8 shows a reciprocal arithmetic circuit according to a second embodiment of this invention. First, the principle of the approximate calculation in the reciprocal arithmetic circuit is explained.

5 The n-bit divisor A after normalized can be given as follows:

$$A = a_1 \cdot (1/2) + a_2 \cdot (1/2)^2 + \dots + a_n \cdot (1/2)^n \quad (9)$$

Further, the upper m-bit data AH and lower (n-m)-bit data AL are given as follows:

$$AH = a_1 \cdot (1/2) + a_2 \cdot (1/2)^2 + \dots + a_m \cdot (1/2)^m \quad (10)$$

$$AL = a_{m+1} \cdot (1/2)^{m+1} + \dots + a_n \cdot (1/2)^n \quad (11)$$

10 The following relation can be set between the divisor A, the upper-bit data AH and the lower-bit data AL:

$$A = AH + AL \quad (12)$$

Assume now that the following equations are satisfied:  $AH1 = AH + (1/2)^m$  (13)

$$AH0 = AH \quad (14)$$

The following condition is satisfied:

$$15 \quad AH0 \leq A < AH1 \quad (15)$$

That is, the divisor A lies between AH0 and AH1 inclusive.

From Eq. (15), the following condition can be set:

$$1/AH1 < 1/A \leq 1/AH0 \quad (16)$$

If, in this case,  $1/AH1 = R01$  and  $1/AH0 = R00$ , then the following condition can be set:

$$20 \quad R01 < 1/A \leq R00 \quad (17)$$

That is, the reciprocal  $1/A$  of the divisor A lies between R01 and R00. R01 is the reciprocal of AH1 or  $[AH0 + (1/2)^m]$ , R00 is the reciprocal of AH0, and  $1/A$  is the reciprocal of A or  $(AH0 + AL)$ . Therefore,  $1/A$  may be approximated on a straight line connecting R01 and R00 and the value thereof can be obtained by a linear function.

25 Based on the coordinate  $[AH0 + (1/2)^m, R01]$  of R01, the coordinate  $(AH0 + AL, 1/A)$  of  $1/A$ , and the coordinate  $(AH0, R00)$  of R00, the following approximate equation representing  $1/A$  can be obtained:

$$1/A = R1 = \frac{AL \cdot R01 + \{(1/2)^m - AL\} \cdot R00}{AL + \{(1/2)^m - AL\}}$$

30

$$R1 = R00 + 2^m \cdot AL \cdot (R01 - R00) \quad \text{--- (18)}$$

35 The reciprocal arithmetic circuit of the second embodiment effects the approximate calculation shown in Eq. (18).

In the reciprocal arithmetic circuit of the second embodiment shown in Fig. 8, a ROM table 31 stores approximation information of reciprocals ( $1/AH$ ) of the upper-bit data AH of divisors A, and approximation information of  $[(1/AH) + (1/2)^m]$ . The ROM table 31 receives the upper m-bit data AH of the divisor A as an address signal, converts the address data AH into the reciprocal ( $1/AH$ ) thereof and then outputs the same. At the same time, it converts the address data AH into the reciprocal

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$$\left[ \frac{1}{AH + (1/2)^m} \right]$$

45

of the data  $[AH + (1/2)^m]$  and outputs the same. That is, the reciprocal ( $1/AH$ ) of the data AH and the reciprocal

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$$\left[ \frac{1}{AH + (1/2)^m} \right]$$

55 of the data  $[AH + (1/2)^m]$  are read out from the ROM 31 at the same time. The two readout reciprocal approximate data are respectively set to R00 ( $\approx 1/AH = AH0$ ) and

$$(\approx \frac{1}{AH + (1/2)^m} = AH1).$$

R01

In this case, R00, R01 and the reciprocal  $1/A$  satisfy the relation of  $R01 < 1/A \leq R00$  as described before.

The reciprocal approximate data R00 read out from the ROM table 31 is supplied to one input terminal of a subtracter circuit 32 and one input terminal of an adder/subtractor circuit 34. On the other hand, the reciprocal approximate data R01 read out from the ROM table 31 is supplied to the other input terminal of the subtracter circuit 32. The subtracter circuit 32 derives a difference (R01-R00) between the reciprocal approximate data R01 and R00. The difference output (R01-R00) of the subtracter circuit 32 is supplied to one input terminal of a multiplier circuit 33. The other input terminal of the multiplier circuit 33 is supplied with the lower (n-m)-bit data AL of the divisor A which is carried by  $2^m$  bits or shifted by m bits to the left or in an upper digit direction. That is, the other input terminal of the multiplier circuit 33 is supplied with  $2^m \cdot AL$ . The multiplier circuit 33 multiplies the output (R01-R00) of the subtracter 32 by  $2^m \cdot AL$  to supply an output of  $2^m \cdot AL \cdot (R01-R00)$  to the other input terminal of the adder/subtractor circuit 34. Then, the adder/subtractor circuit 34 adds R00 to  $2^m \cdot AL \cdot (R01-R00)$ , and outputs an addition result  $[R00 + 2^m \cdot (AL \cdot R01 - R00)]$  as the approximation R1 of the reciprocal  $1/A$ .

Fig. 9 is a flowchart showing the approximate calculation process of the reciprocal arithmetic circuit according to the second embodiment shown in Fig. 8. That is, memory information of the ROM table 31 is searched for according to the upper m-bit data AH of the divisor A used as an address. As the result of this searching operation, the approximate reciprocal  $(1/AH) = (1/AH0)$  of the data AH and the approximate reciprocal

$$[\frac{1}{AH + (1/2)^m}] = (1/AH1)$$

of the data  $[AH + (1/2)^m]$  are obtained at the same time (steps S31 and S32). Next,  $1/AH0$  and  $1/AH1$  are substituted for R00 and R01 (step S33), and then the approximate calculation shown in Eq. (18) is made (step S34).

Like the first embodiment, in the second embodiment, the multiplier circuit 33 is required to effect only one multiplication of (R01-R00) and  $2^m \cdot AL$  in order to make the approximate calculation. As described before, the multiplication of  $2^m \cdot AL$  can be obtained by shifting the lower-bit data AL to the left by m bits.

Further, in the second embodiment, since the precalculation based on the approximate reciprocal data R01 and lower-bit data AL is made by use of the subtracter circuit 32 and multiplier circuit 33, the approximate calculation for making the approximate reciprocal data R00 nearer to the reciprocal  $1/A$  of the divisor A can be made only by an addition by means of the adder/subtractor circuit 34. In this way, in the second embodiment, the reciprocal calculation can be made at a high speed by use of a hardware simple in construction.

Fig. 10 shows a modification of the reciprocal arithmetic circuit according to the second embodiment shown in Fig. 8. Like the second embodiment, the reciprocal arithmetic circuit of Fig. 10 derives the approximation R1 of a reciprocal  $1/A$  by use of two approximate reciprocal data R00 and R01 generated from a ROM table. However, unlike the second embodiment in which the approximate calculation is made based on Eq. (18), the following approximation calculation is used:

$$R1 = R00 \cdot (1 - 2^m \cdot AL) + 2^m \cdot AL \cdot R01 \quad (24)$$

It is easily understood that Eq. (24) is a modification of Eq. (18).

In Fig. 10, the ROM table 43 stores approximation information of reciprocals  $(1/AH)$  of upper-bit data AH of divisors A.

An adder circuit 41 and a selector 42 are provided in the preceding stage of the ROM table 43 and data AH and  $AH + 1$  are selectively supplied to the ROM table 43 by means of the adder circuit 41 and selector 42. The ROM table converts the data AH into the reciprocal  $(1/AH = R00)$  thereof and outputs the same in response to the upper m-bit data AH of the divisor A supplied as an address signal. In contrast, it converts the data  $AH + (1/2)^m$  into the reciprocal

$$\left( \frac{1}{AH + (1/2)^m} = R01 \right)$$

5 thereof and outputs the same in response to the data  $AH + (1/2)^m$  supplied as an address signal.

The output R00 or R01 of the ROM table 43 is supplied to one input terminal of a multiplier circuit 46. A subtracter circuit 44 and a selector 45 are provided in the preceding stage of the other input terminal of the multiplier circuit 46. The subtracter circuit 44 receives the lower m-bit data AL of the divisor A which is shifted by m bits to the left and derives a subtraction result of  $(1-2^m \cdot AL)$ . The output  $(1-2^m \cdot AL)$  of the subtracter 44 is supplied to one input terminal of the selector 45. The subtracter 45 also receives the lower-bit data AL which is shifted by m bits to the left at the other input terminal thereof. The selector 45 selectively supplies  $(1-2^m \cdot AL)$  or  $2^m \cdot AL$  to the other input terminal of the multiplier circuit 46.

The multiplier circuit 46 multiplies the output R00 (or R01) of the ROM table 43 by the output  $(1-2^m \cdot AL)$  (or  $2^m \cdot AL$ ) to supply the multiplication result  $R00 \cdot (1-2^m \cdot AL)$  or  $2^m \cdot AL \cdot R01$  to a first input terminal of an adder/subtractor circuit 47. An output of the adder/subtractor circuit 47 is fed back to a second input terminal thereof via an accumulator 48. Therefore, the adder/subtractor circuit 47 adds together  $R00 \cdot (1-2^m \cdot AL)$  and  $2^m \cdot AL \cdot R01$  and outputs the addition result  $R00 \cdot (1-2^m \cdot AL) + 2^m \cdot AL \cdot R01$  as the approximation R1 of the reciprocal  $1/A$ .

As described above, in the reciprocal arithmetic circuit of Fig. 10, the first data  $R00 \cdot (1-2^m \cdot AL)$  is derived in the first operation cycle and the second data  $2^m \cdot AL \cdot R01$  is derived and the first and second data are added together in the second operation cycle.

Fig. 11 is a flowchart showing the approximation calculation process of the reciprocal arithmetic circuit of Fig. 10.

#### 1) First Cycle

First, data AH is supplied to the ROM table 43 and the reciprocal approximate data  $1/AH$  of the data AH or R00 is derived (steps S41 to S43). At the same time, a subtraction of  $[1-(2^m \cdot AL)]$  is effected by means of the subtracter circuit 44.

Then, the multiplier circuit 46 multiplies the output R00 of the ROM table 43 by the output  $(1-2^m \cdot AL)$  of the subtracter circuit 44. The multiplication result is added to "0" by means of the adder/subtractor circuit 47 and then stored as R10 into the accumulator 48 (step S44).

#### 2) Second Cycle

First, address data  $AH + 1$  is input to the ROM table 43 to read out

$$\frac{1}{AH + (1/2)^m}$$

or R01 from the ROM table 43 (steps S45 to S47).

Then, the multiplier circuit 46 multiplies the output of the ROM table 43 by the output  $2^m \cdot AL$  of the selector 45.

After this, the adder/subtractor circuit 47 adds the output  $2^m \cdot AL \cdot R01$  of the multiplier circuit 46 to the data R10 or  $R00 \cdot (1-2^m \cdot AL)$  stored in the accumulator 48 (step S48).

By effecting the above two operation cycles, the approximate R1 of the reciprocal  $1/A$  can be derived.

Figs. 12A and 12B show the approximate calculation characteristics of the second embodiment shown in Fig. 8. That is, Fig. 12A shows the relation between the divisor A and the reciprocal  $1/A$  thereof in a case where the divisor A increases in the step of  $(1/2)^m$ , and the line L1 indicates the ideal relation therebetween and the line L3 indicates the relation obtained by the approximate calculation by the reciprocal arithmetic circuit according to the second embodiment. The modification of the second embodiment shown in Fig. 10 also has the same approximate calculation characteristics as shown by the line L3. Fig. 12B shows the magnitude of an error of the reciprocal approximation obtained by use of the reciprocal arithmetic circuit of the second embodiment. Figs. 13A and 13B are enlarged views respectively corresponding to Figs. 12A

and 12B and show the approximate calculation characteristics in one step of variation in the divisor A or in that range of the divisor A which lies between  $(1/2) + (1/2)^m$  and  $1/2$ .

In a reciprocal arithmetic circuit according to a third embodiment to be described below, the function of detecting an error caused by the approximate calculation made in the first and second embodiments and correcting the reciprocal approximation R1 is further added.

Fig. 14 schematically shows the reciprocal arithmetic circuit according to the third embodiment. As described with reference to Fig. 7B, the magnitude of an error in the reciprocal approximation R depends on the lower-bit data AL. For this reason, in the third embodiment, the range of the lower-bit data AL for the error of 2 [LSB] or more is previously stored into a ROM table 51 and the reciprocal approximation R1 is corrected when the value of the lower-bit data AL of the divisor A lies in the range stored in the ROM table 51. The determination whether or not the value of the lower-bit data AL of the divisor A lies in the error occurrence range stored in the ROM table 51 is made by means of a comparison circuit 53. Further, the correction process for the reciprocal approximation R1 is effected by adding or subtracting a correction value D to or from R1 by use of adder/subtractor circuit 55.

Fig. 15 shows the detail construction obtained by applying the third embodiment to the first embodiment shown in Fig. 4. As shown in Fig. 15, an error correction circuit 61 includes a ROM table 59 and a comparison circuit 60. The ROM table 59 stores the error occurrence range of the lower-bit data AL which is determined based on the error characteristics (see Figs. 6B and 7B) of the reciprocal arithmetic circuit of the first embodiment.

That is, the ROM table 59 stores that value AL1 of the lower-bit data which causes an error of 2 [LSB] and that value AL2 of the lower-bit data which causes an error of 3 [LSB] together with the corresponding input upper-bit data AH. The comparison circuit 60 compares the each value of the lower-bit data AL1, AL2 output from the ROM table 59 with the value of the lower-bit data AL of the divisor A to detect the error occurrence range to which the lower-bit data AL belongs.

For example, when the comparator 60 detects that the lower-bit data AL belongs to the range of  $0 \leq AL \leq AL1$ , it generates the correction value D of "0" since the magnitude of the error is less than 1 [LSB]. Further, when it is detected that the lower-bit data AL lies in the range of  $AL1 \leq AL < AL2$ , the comparator 60 generates the correction value D of "-1" since the magnitude of the error lies between 1 [LSB] and 2 [LSB] and it is necessary to make the error less than 1 [LSB]. when it is detected that the lower-bit data AL lies in the range of  $AL2 \leq AL$ , the comparator 60 generates the correction value D of "-2" since the magnitude of the error is more than 2 [LSB].

Next, the operation of the reciprocal arithmetic circuit of Fig. 15 is explained with reference to a flowchart shown in Fig. 16. First, the upper-bit data AH of the divisor A is input as an address signal to the ROM table 21 to read out  $(1/AH)^2$  from the ROM table 21 (steps S51 and S52). Likewise, the upper-bit data AH is input to the ROM table 59 to read out the value AL1, AL2, ..., ALd of the lower-bit data which may cause an error from the ROM table 59 (step S53). In this case, AL1 is the minimum value of the lower-bit data AL which causes an error of 2 [LSB], AL2 is the minimum value of the lower-bit data AL which causes an error of 3 [LSB] and ALd is the minimum value of the lower-bit data AL which causes an error of d + 1 [LSB].

The comparator circuit 60 compares the value AL1, AL2, ..., ALd with the lower-bit data AL of the divisor A to determine the error occurrence range ( $0 \leq AL < AL1$ ,  $AL1 \leq AL < AL2$ , or  $ALd \leq AL$ ) to which the lower-bit data AL belongs (steps S541 to S54d). Then, in order to make the error of the approximate calculation less than 1 [LSB], the correction value D is determined according to the error occurrence range to which AL belongs (steps S551 to S55d).

Next, a calculation of  $R0 \cdot (AH - AL)$  is made by an operation circuit 23 with the output  $(1/AH)^2$  of the ROM table 21 used as R0 (steps S56 and S57).

Figs. 17A to 17C show the characteristics of the approximate calculation operation of the reciprocal arithmetic circuit of Fig. 15. That is, the approximate calculation characteristic prior to the correction process is shown by a line L2 and the ideal characteristic is shown by a line L1 in Fig. 17A. Fig. 17B shows the error characteristic prior to the correction process and Fig. 17C shows the error characteristic after the correction process. As is clearly seen from Fig. 17C, the error after the correction process becomes less than 1 [LSB] and the approximate reciprocal R1 becomes equal to the true reciprocal  $1/A$  obtained in the fraction cut-off mode.

Figs. 18A to 18C show the characteristics of the approximate calculation operation of the reciprocal arithmetic circuit obtained by applying the third embodiment of Fig. 14 to the reciprocal arithmetic circuit of the second embodiment shown in Fig. 8. That is, the approximate calculation characteristic prior to the correction process is shown by a line L3 and the ideal characteristic is shown by a line L1 in Fig. 18A. Fig. 18B shows the error characteristic prior to the correction process and Fig. 18C shows the error characteris-



tic after the correction process. As is clearly seen from Fig. 18C, the error after the correction process can be made less than 1 [LSB] also in a case where the correction process of the third embodiment is applied to the second embodiment.

$$R1 = 1/A = \frac{1}{AH+AL} = \frac{1}{AH^3+AL^3} \cdot (AH^2-AH \cdot AL+AL^2)$$

Assuming that  $AH^3 \gg AL^3$ , then the following expression can be obtained:

$$R1 \approx \frac{1}{AH^3} \cdot (AH^2 + AH \cdot AL + AL^2) \quad (19)$$

In the fourth embodiment, the approximate calculation shown in Eq. (19) is effected according to the flowchart shown in Fig. 20 so as to derive an approximation R1.

A reciprocal arithmetic circuit of the fourth embodiment shown in Fig. 19 includes a ROM table 71, selectors 72 to 74, a multiplier circuit 75, an adder/subtractor circuit 76 and an accumulator 77.

The ROM table 71 stores approximation information of the cubes  $(1/AH)^3$  of the reciprocals of the upper-bit data AH of divisors A. In the reciprocal arithmetic circuit, the upper-bit data AH is first selected by means of the selectors 72 and 73, a calculation of  $(AH \cdot AH + 0)$  is made by the multiplier circuit 75 and adder/subtractor circuit 76, and the calculation result is stored as ACC0 into the accumulator 77. Next, the lower-bit data AL is selected by means of the selectors 72 and 73 and an output of the accumulator 77 is selected by means of the selector 74. As a result, an operation of  $(AL \cdot AL + ACC0)$  is effected by use of the multiplier circuit 75 and the adder/subtractor circuit 76, and the operation result is stored as ACC0 into the accumulator 77. Then, the upper-bit data AH is selected by means of the selector 72, the lower-bit data AL is selected by means of the selector 73, and an output of the accumulator 77 is selected by means of the selector 74. As a result, an operation of  $(ACC0 - AH \cdot AL)$  is effected by use of the multiplier circuit 75 and adder/subtractor circuit 76 and  $(AH^2 + AL^2 - AH \cdot AL)$  is newly stored as ACC0 into the accumulator 77. Next, an output of  $(1/AH)^3$  of the ROM table 71 is selected by means of the selector 72 and an output of the accumulator 77 is selected by means of the selector 73. Therefore, an operation of  $ACC0 \cdot (1/AH)^3 + 0$  is effected by means of the multiplier circuit 75 and the adder/subtractor circuit 76 and the operation result is stored as ACC0 into the accumulator 77 again. As a result, the same operation result as that of Eq. (19) can be obtained in the accumulator 77.

Fig. 21 shows the relation between the bit number n of the divisor A and the bit number m of the upper-bit data AH, and in the fifth embodiment,  $m=3$  bits when  $n=8$  bits, for example. That is, in the fourth embodiment, it becomes possible to reduce the number of bits to be input to the ROM table in comparison with the approximation process using the full-bit method and Newton's method mentioned before, thereby making it possible to reduce the memory capacity of the ROM table.

Fig. 22 shows a reciprocal arithmetic circuit according to the fifth embodiment of this invention. First, the principle of the calculation of the approximation R1 in the fifth embodiment is explained.

$$R1 = 1/A = \frac{1}{AH+AL} = \frac{1}{AH^4+AL^4} \cdot (AH-AL) \cdot (AL^2+AL^2)$$

Assuming that  $AH^4 \gg AL^4$ , the following expression can be obtained:

$$R1 \approx (1/AH)^4 \cdot (AH-AL) \cdot (AH^2 + AL^2) \quad (20)$$

In the fifth embodiment, the approximation R1 of the reciprocal  $1/A$  can be derived by effecting the approximate calculation of Eq. (20) according to the flowchart of Fig. 23.

The reciprocal arithmetic circuit according to the fifth embodiment shown in Fig. 22 includes a ROM table 81, selectors 82 to 84, a multiplier circuit 85, an adder/subtractor circuit 86, and accumulators 87 and 88.

The ROM table 81 stores approximation information of reciprocals  $(1/AH)^4$  of the upper-bit data AH of divisors A to the fourth power. In the reciprocal arithmetic circuit, the upper-bit data AH is first selected by means of the selectors 82 and 83, a calculation of  $AH^2$  is made by the multiplier circuit 85, and  $AH^2$  is stored as ACC0 into the accumulator 87. Next, the lower-bit data AL is selected by means of the selectors 82 and 83, a calculation of  $AL^2$  is made by the multiplier circuit 85, and  $AL^2$  is stored as ACC1 into the accumulator 88. Then, an operation of  $(ACC0 + ACC1)$  is effected by use of the adder/subtractor circuit 86 and  $(AH^2 + AL^2)$  is newly stored as ACC0 into the accumulator 87. Next, an operation of  $(AH-AL)$  is effected by use of the adder/subtractor circuit 86 and the operation result is stored into the accumulator 88. Next, an

output of  $(1/AH)^4$  is read out from the ROM table 81 and then an operation of  $ACC1 \cdot (1/AH)^4$  is effected by means of the multiplier circuit 85 and the operation result is newly stored as ACC1 into the accumulator 88 again. Then, a multiplication ( $ACC1 \cdot ACC0$ ) of data in the accumulators 87 and 88 is effected by means of the multiplier circuit 85. As a result, the same operation result as that of Eq. (20) can be obtained in the accumulator 88.

Fig. 24 shows the relation between the bit number  $n$  of the divisor  $A$  and the bit number  $m$  of the upper-bit data  $AH$ , and in the fifth embodiment,  $AH=2$  bits when  $n=8$  bits, for example. That is, in the fifth embodiment, it becomes possible to reduce the number of bits to be input to the ROM table in comparison with the approximation calculation process using the full-bit method and Newton's method mentioned before, thereby making it possible to reduce the memory capacity of the ROM table.

As is clearly understood by comparing Figs. 21 and 24, the memory capacity of the ROM table for generating  $(1/AH)^4$  can be made smaller than that of the ROM table for generating  $(1/AH)^3$ . This is because the converting precision of the approximate calculation shown in Eq. (20) is higher than that of the approximate calculation shown in Eq. (19)  $(1/AH)^3$ .

As described above, according to this invention, a reciprocal arithmetic circuit in which the hardware can be made simple and whose operation speed and operation precision are enhanced can be obtained.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

## 20 Claims

1. A reciprocal arithmetic circuit comprising:  
conversion table means (21) for storing approximate information items corresponding to the reciprocals  $[(1/AH)^2]$  of the squares of upper-bit data  $AH$  of divisors  $A$  and converting the upper-bit data  $AH$  supplied as an address into the approximation of the squared reciprocal  $[(1/AH)^2]$  and outputting the approximation;  
subtractor means (22) for deriving a difference  $(AH-AL)$  between the upper-bit data  $AH$  and lower-bit data  $AL$  of the divisor  $A$ ; and  
multiplier means (23) connected to receive an output  $[(1/AH)^2]$  of said conversion table means (21) and an output  $(AH-AL)$  of said subtractor means (22), for deriving the product thereof to make the output  $[(1/AH)^2]$  of said conversion table means more nearly equal to the reciprocal  $1/A$  of the divisor  $A$ .

2. A reciprocal arithmetic circuit according to claim 1, characterized in that said conversion means (21) includes a ROM.

3. A reciprocal arithmetic circuit according to claim 1, further comprising an error occurrence range storing table (51) for storing error occurrence ranges of the lower-bit data  $AL$  corresponding to the respective upper-bit data  $AH$  and outputting the error occurrence range of the lower-bit data  $AL$  corresponding to the upper-bit data  $AH$  when the upper-bit data  $AH$  is supplied as an address, an error component which is included in the approximation output from said conversion table means (21) being larger than a predetermined value in each of the error occurrence ranges; and correction means (53) for determining whether or not the lower-bit data  $AL$  of the divisor  $A$  lies in the error occurrence range of the lower-bit data  $AL$  output from said error occurrence range storing table (51) and correcting the output of said multiplier means (23) upon detecting that the lower-bit data  $AL$  of the divisor  $A$  lies in the error occurrence range.

4. A reciprocal arithmetic circuit comprising: conversion table means (31; 43) for storing approximation information of reciprocals  $1/AH$  of the upper-bit data  $AH$  of divisors  $A$  and converting the upper-bit data  $AH$  into a first reciprocal  $1/AH$  and a second reciprocal

$$\frac{1}{AH + (1/2)^m}$$

when the upper-bit data is supplied as an address and outputting the same; and approximate calculation means (32 to 34; 46 to 48) for proportionally dividing a line connecting the first reciprocal  $1/AH$  and the second reciprocal

$$\frac{1}{AH + (1/2)^m}$$

based on the lower-bit data AL of the divisor A in order to make the first reciprocal  $1/AH$  output from said conversion table means (31; 43) more nearly equal to the reciprocal  $1/A$  of the divisor A.

5. A reciprocal arithmetic circuit according to claim 4, characterized in that said conversion means (31; 43) includes a ROM.

6. A reciprocal arithmetic circuit according to claim 4, characterized in that said approximate calculation means (32 to 34) effects an operation of

$$(1/AH) + 2^m \cdot AL \cdot \left\{ \frac{1}{AH + (1/2)^m} - 1/AH \right\}$$

when the bit number of the upper-bit data AH is m.

7. A reciprocal arithmetic circuit according to claim 6, characterized in that said approximate calculation means (32 to 34) includes subtracter means (32) for deriving a difference

$$\left\{ \frac{1}{AH + (1/2)^m} - 1/AH \right\}$$

between the second reciprocal

$$\left( \frac{1}{AH + (1/2)^m} \right)$$

and the first reciprocal  $1/AH$ ; multiplier means (33) having a first input terminal supplied with an output of said subtracter means (32) and a second input terminal supplied with the lower-bit data AL of the divisor A shifted by m bits in an upper digit direction, for multiplying the data received at the first and second input terminals by each other; and adding means (34) for adding together an output of said multiplier means (33) and the first reciprocal  $1/AH$ .

8. A reciprocal arithmetic circuit according to claim 4, characterized in that said approximate calculation means (46 to 48) effects an operation of

$$(1/AH) \cdot (1 - 2^m \cdot AL) + 2^m \cdot AL \cdot \left( \frac{1}{AH + (1/2)^m} \right)$$

when it is assumed that the bit number of the upper-bit data AH is m.

9. A reciprocal arithmetic circuit according to claim 4, further comprising an error occurrence range storing table (51) for storing error occurrence ranges of the lower-bit data AL corresponding to the respective upper-bit data AH and outputting the error occurrence range of the lower-bit data AL corresponding to the upper-bit data AH when the upper-bit data AH is supplied as an address, an error component which is included in the approximation output from said conversion table means being larger than a predetermined value in each of the error occurrence ranges; and correction means (53, 55) for determining whether or not the lower-bit data AL of the divisor A lies in the error occurrence range of the lower-bit data AL output from said error occurrence range storing table (51) and correcting the output of said approximation calculation means (32 to 34; 46 to 48) upon detecting that the lower-bit data AL of the divisor A lies in the error occurrence range.

10. A reciprocal arithmetic circuit comprising:  
conversion table means (71) for storing approximate information items corresponding to the reciprocals  $[(1/AH)^3]$  of the cubes of upper-bit data AH of divisors A and converting the upper-bit data AH supplied as an address into the approximation of the cube  $[(1/AH)^3]$  of the reciprocal thereof and outputting the approximation;  
pre-processing means (75, 76, 77) for effecting a calculation of  $(AH^2 - AH \cdot AL + AL^2)$  based on the upper-bit data AH and lower-bit data AL of the divisor A; and  
approximation calculation means (75) for multiplying an output of said conversion table means (71) by an

output of said pre-processing means (75, 76, 77) to make the output  $(1/AH)^3$  of said conversion table means more nearly equal to the reciprocal  $1/A$  of the divisor A.

11. A reciprocal arithmetic circuit comprising:

- conversion table means (81) for storing approximate information items corresponding to the reciprocals  $[(1/AH)^4]$  of upper-bit data AH of divisors A to the fourth power and converting the upper-bit data AH supplied as an address into the approximation of the reciprocal  $[(1/AH)^4]$  of AH to the fourth power and outputting the approximation;
- pre-processing means (85, 86, 87, 88) for effecting a calculation of  $(AH-AL) \cdot (AH^2 + AL^2)$  based on the upper-bit data AH and lower-bit data AL of the divisor A; and
- approximation calculation means (85) for multiplying an output of said conversion table means (81) by an output of said pre-processing means (85, 86, 87, 88) to make the output  $(1/AH)^4$  of said conversion table means (81) more nearly equal to the reciprocal  $1/A$  of the divisor A.

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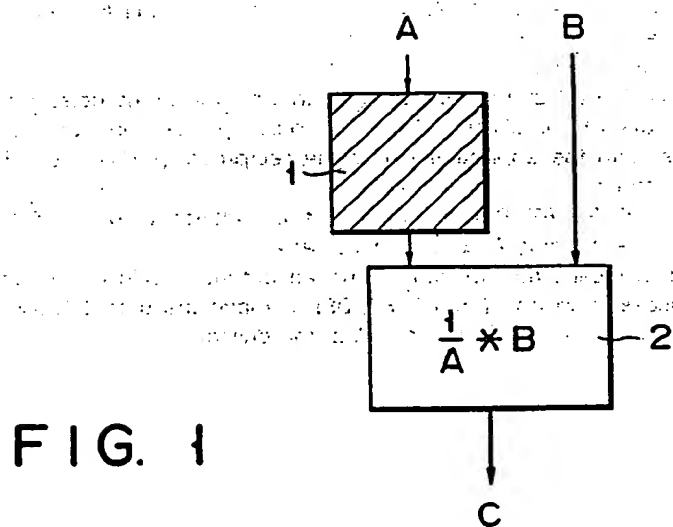


FIG. 1

| INPUT/OUTPUT<br>BIT WIDTH OF ROM | ROM SIZE     | LOWEST POSSIBLE<br>LOOP NUMBER N |
|----------------------------------|--------------|----------------------------------|
| 2                                | 8            | 3                                |
| 4                                | 64           | 2                                |
| 6                                | 384          | 2                                |
| 8                                | 2K (256 x 8) | 1                                |
| 10                               | 10K          | 1                                |
| 12                               | 48K          | 1                                |
| 14                               | 224K         | 1                                |
| 16                               | 1M           | 1                                |

FIG. 3

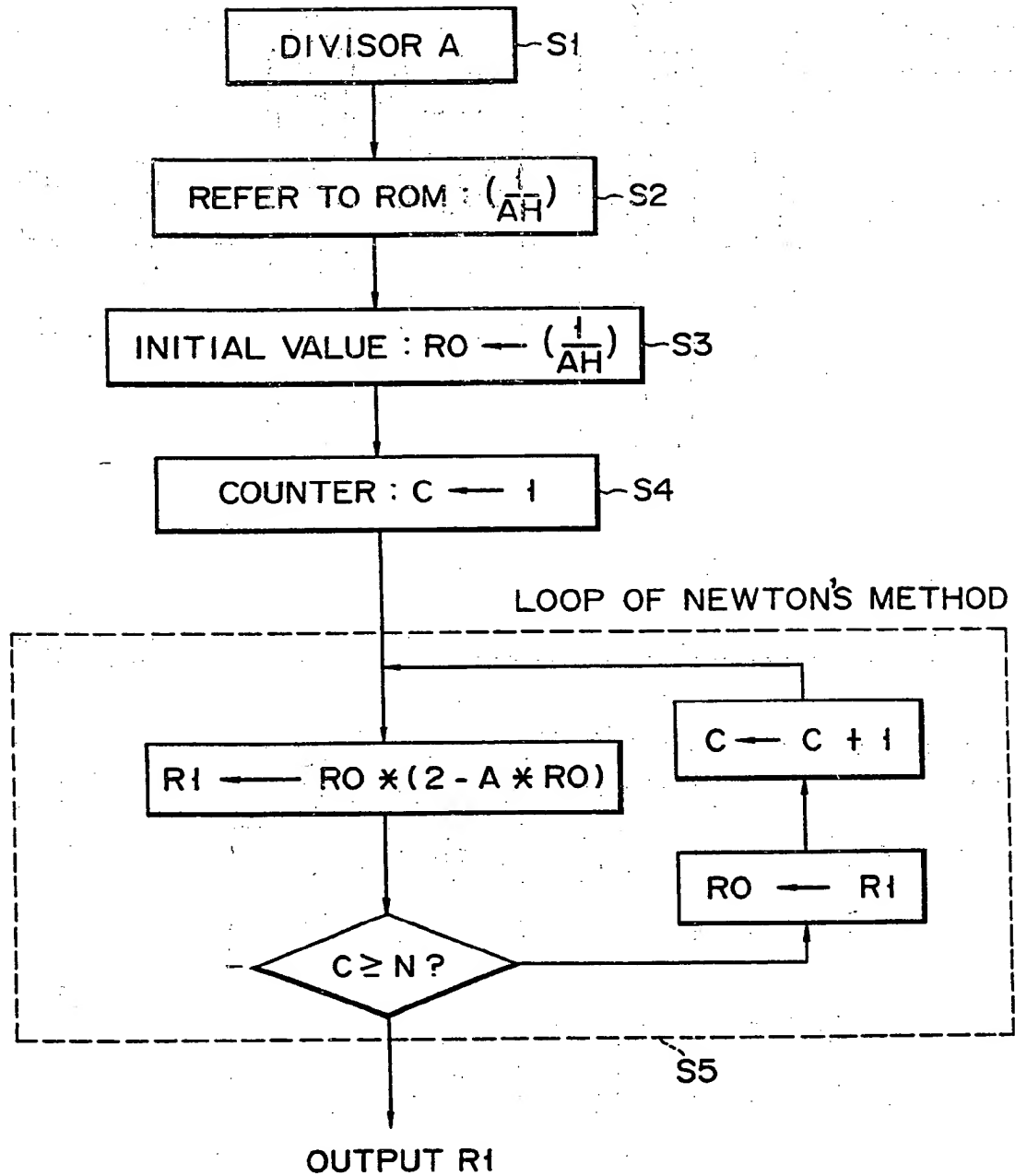


FIG. 2

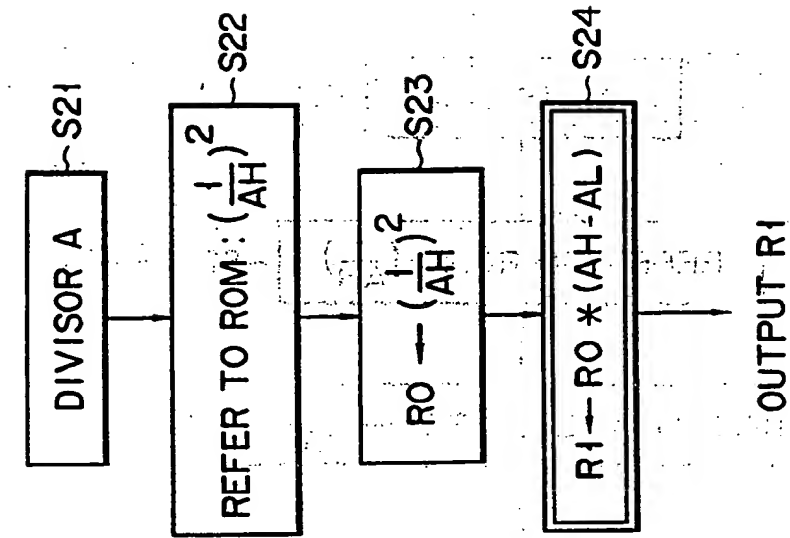


FIG. 5

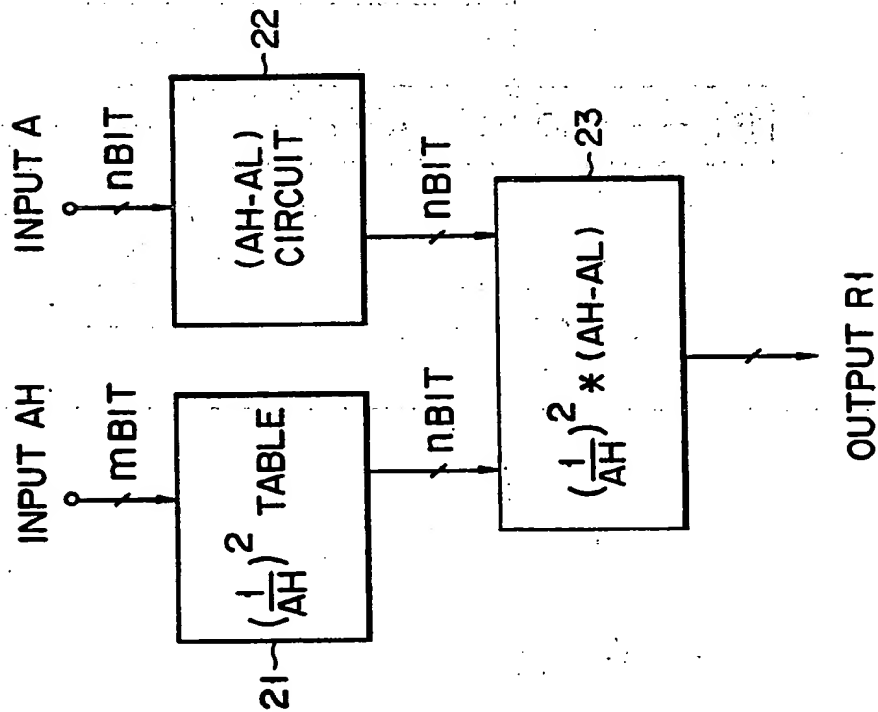


FIG. 4

FIG. 6A

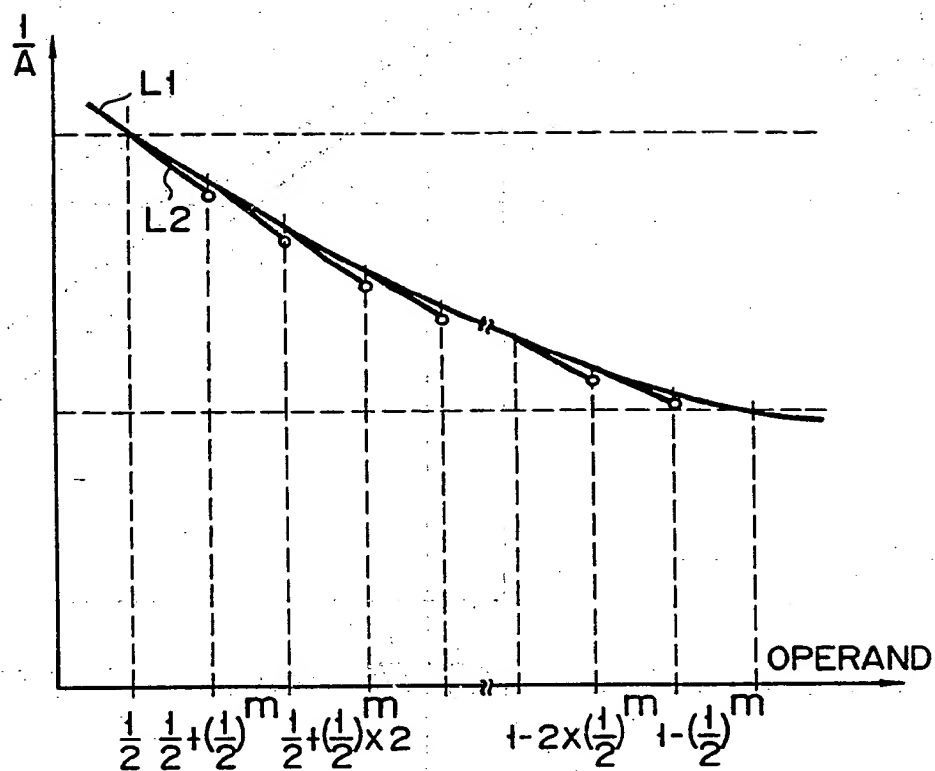


FIG. 6B

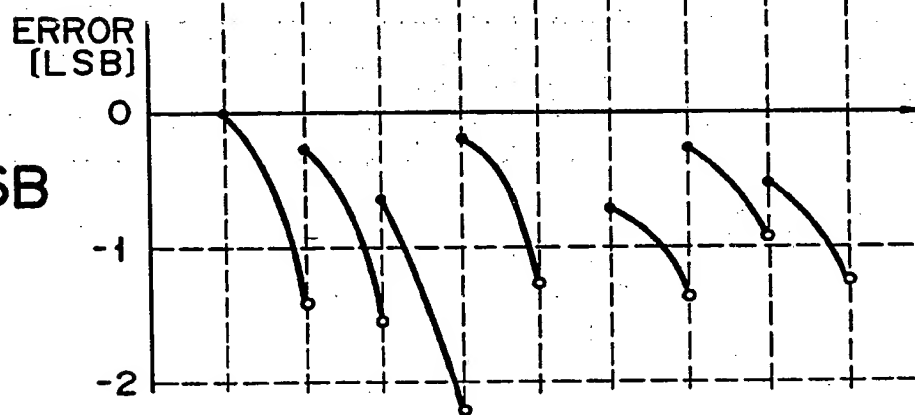




FIG. 7A

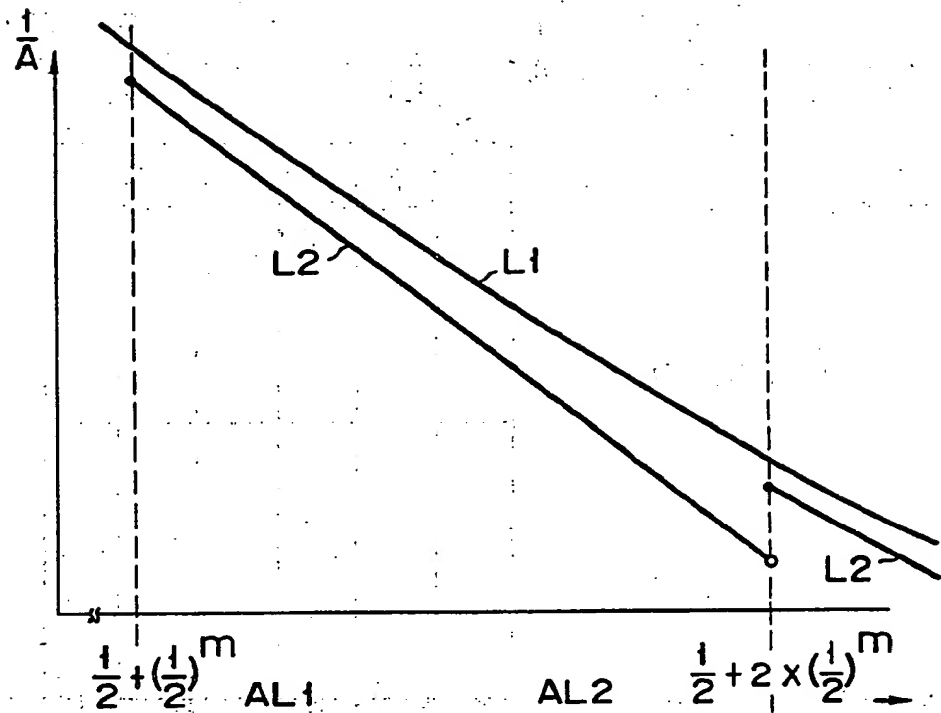
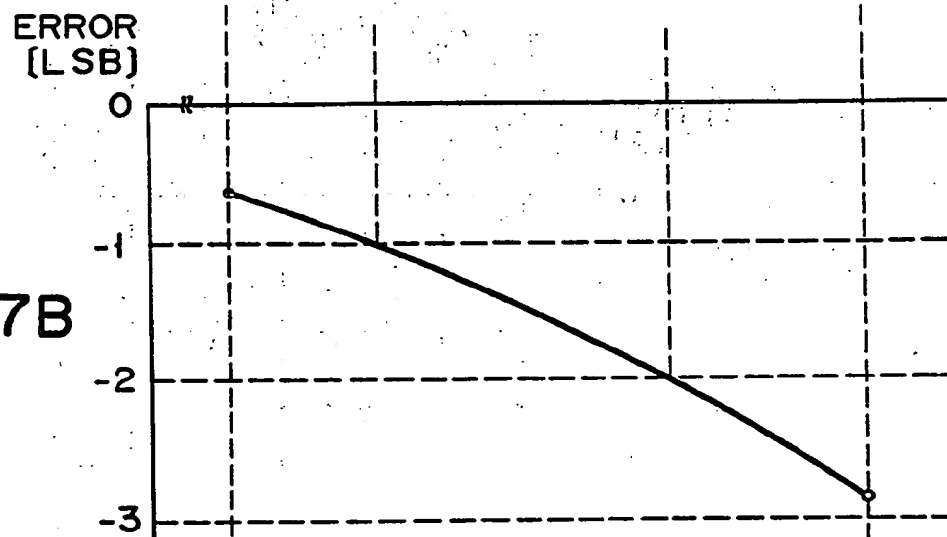


FIG. 7B



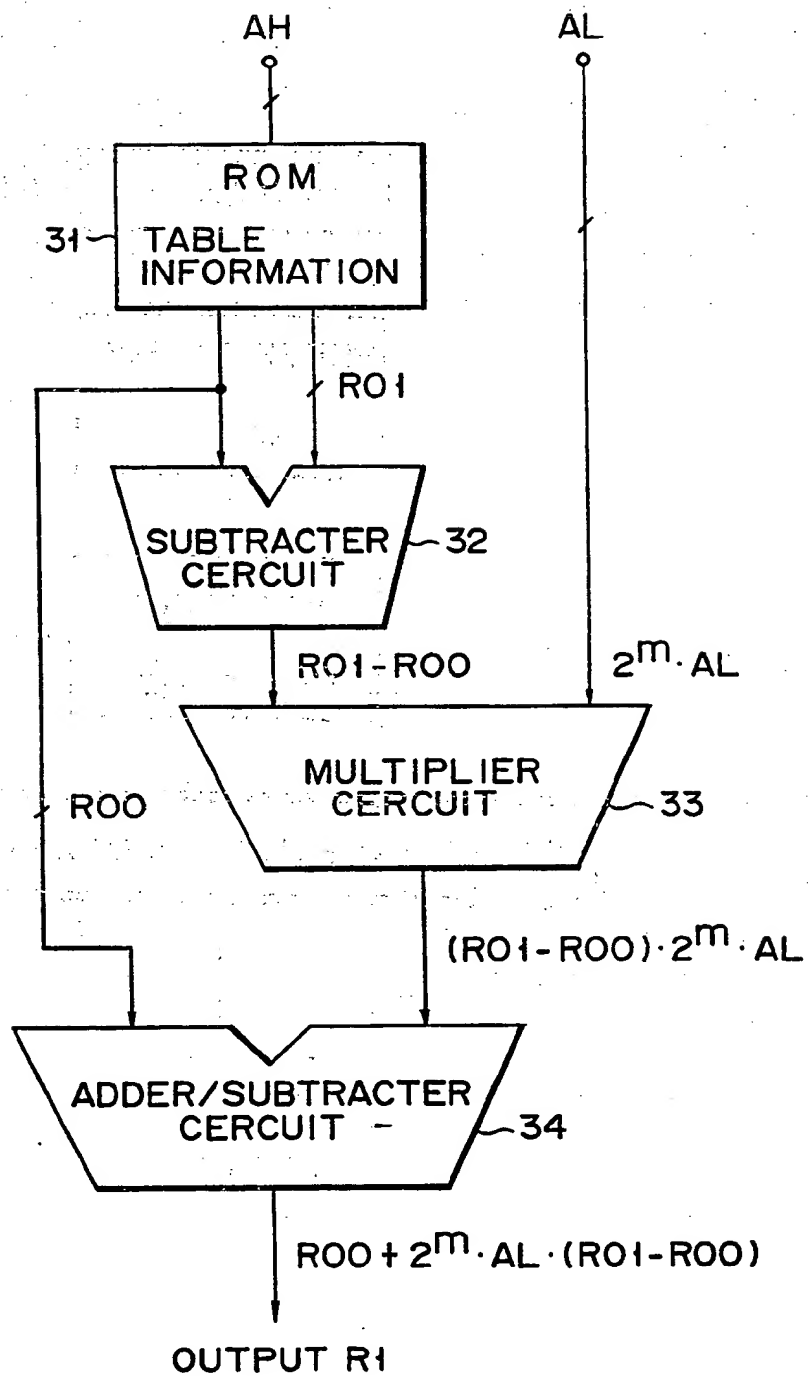


FIG. 8

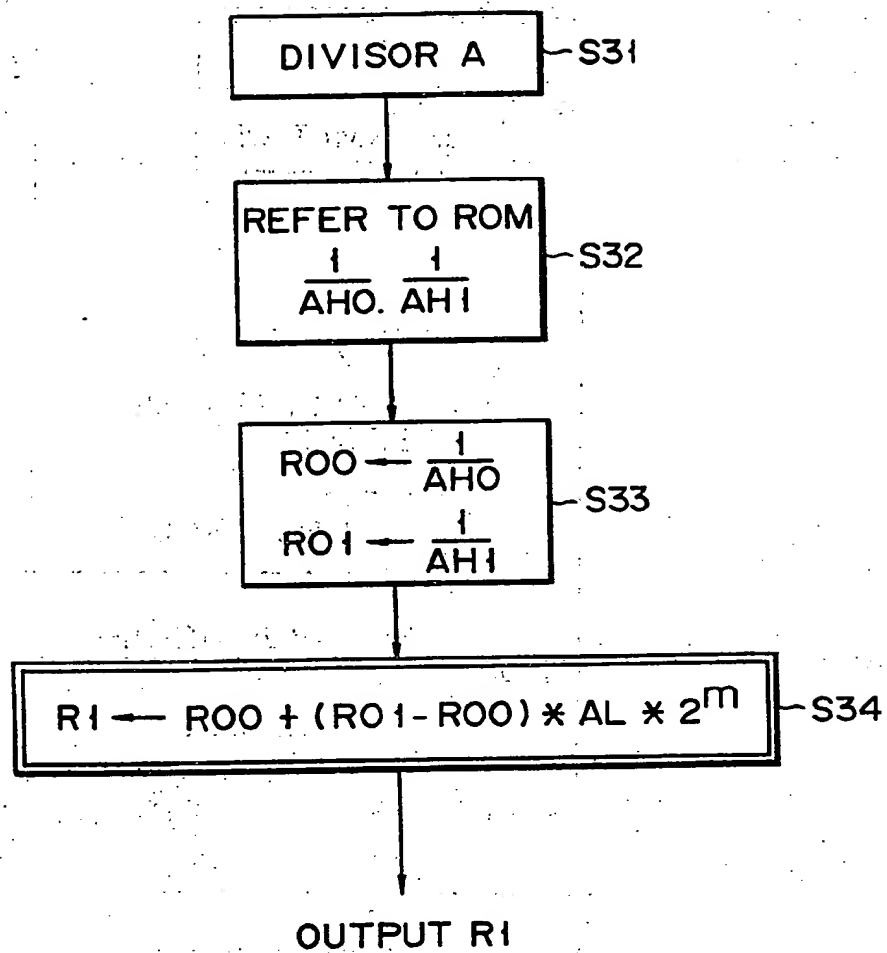


FIG. 9

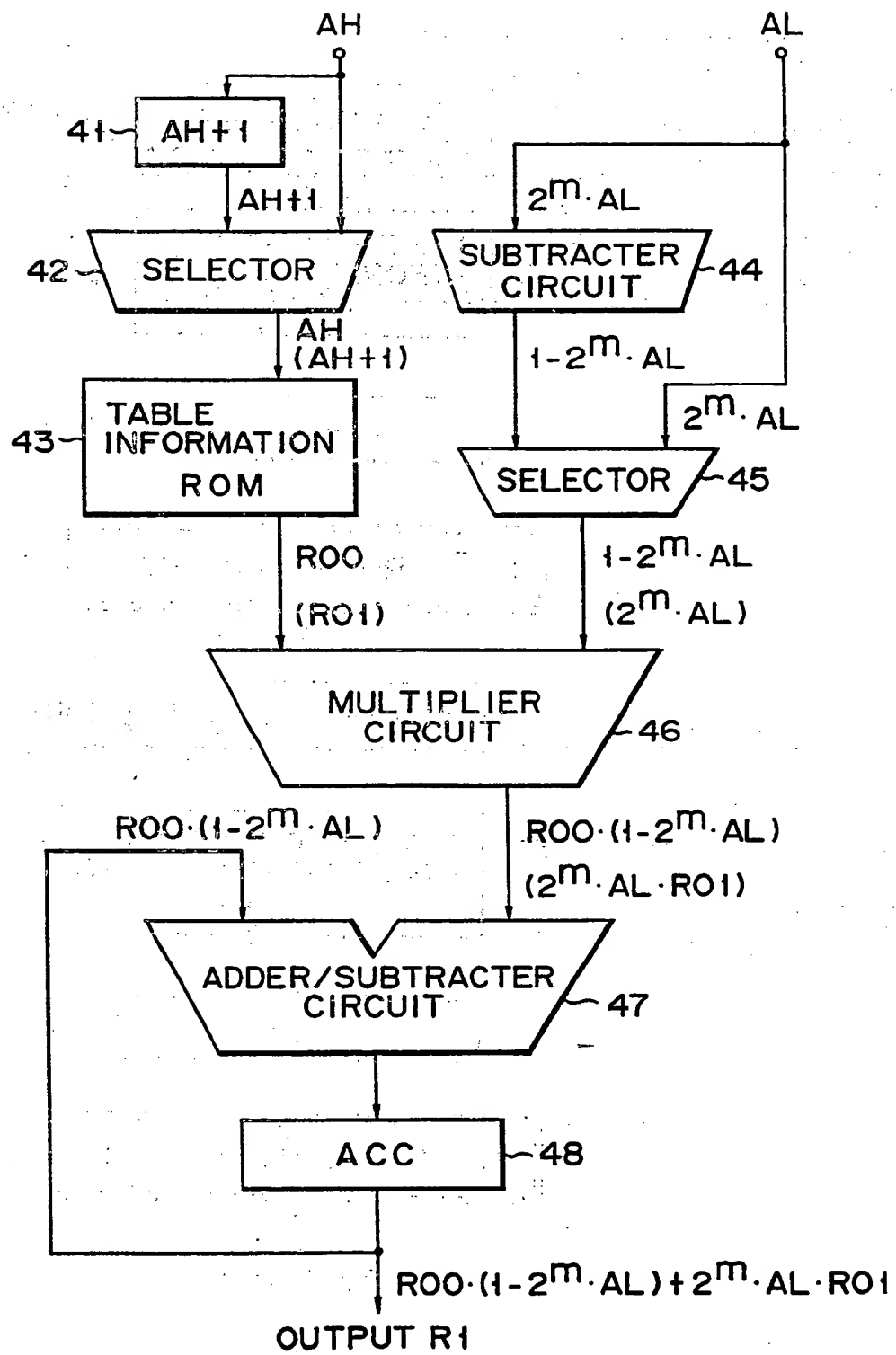


FIG. 10

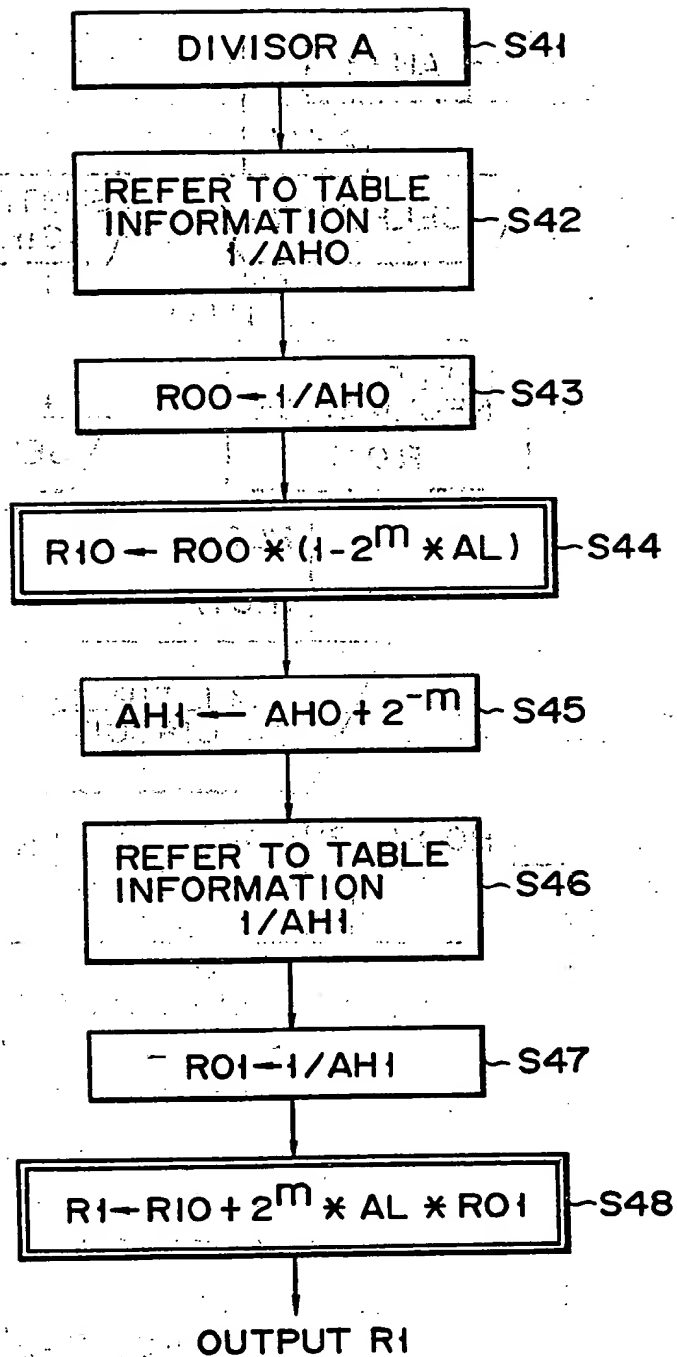


FIG. 11

FIG.12A

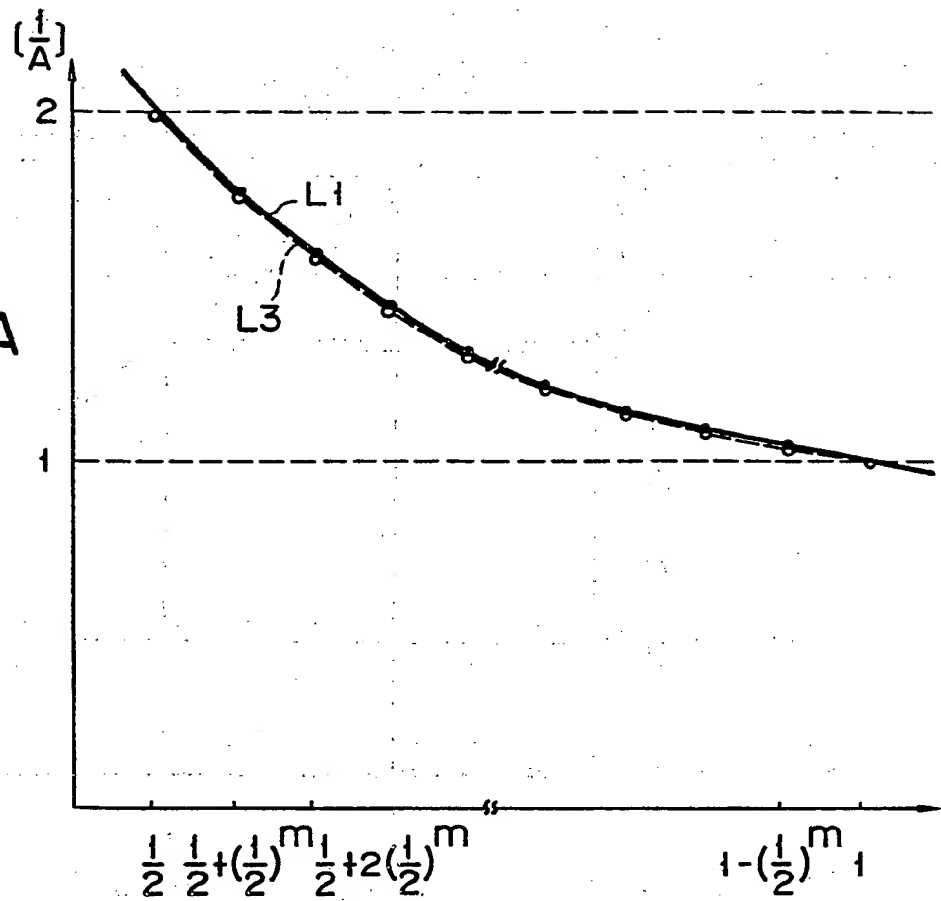
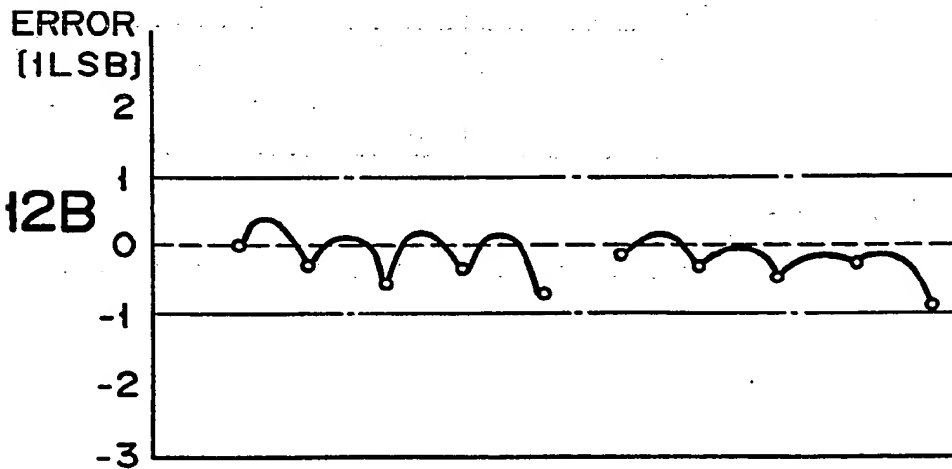
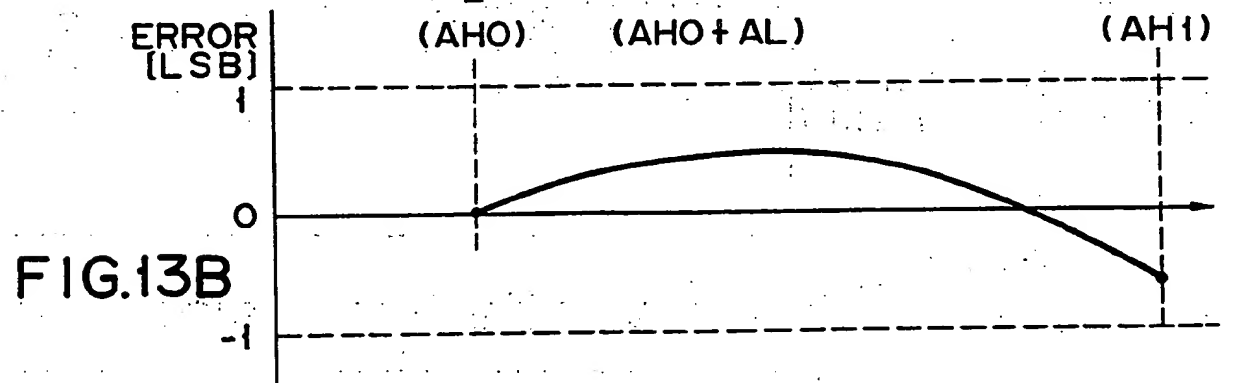
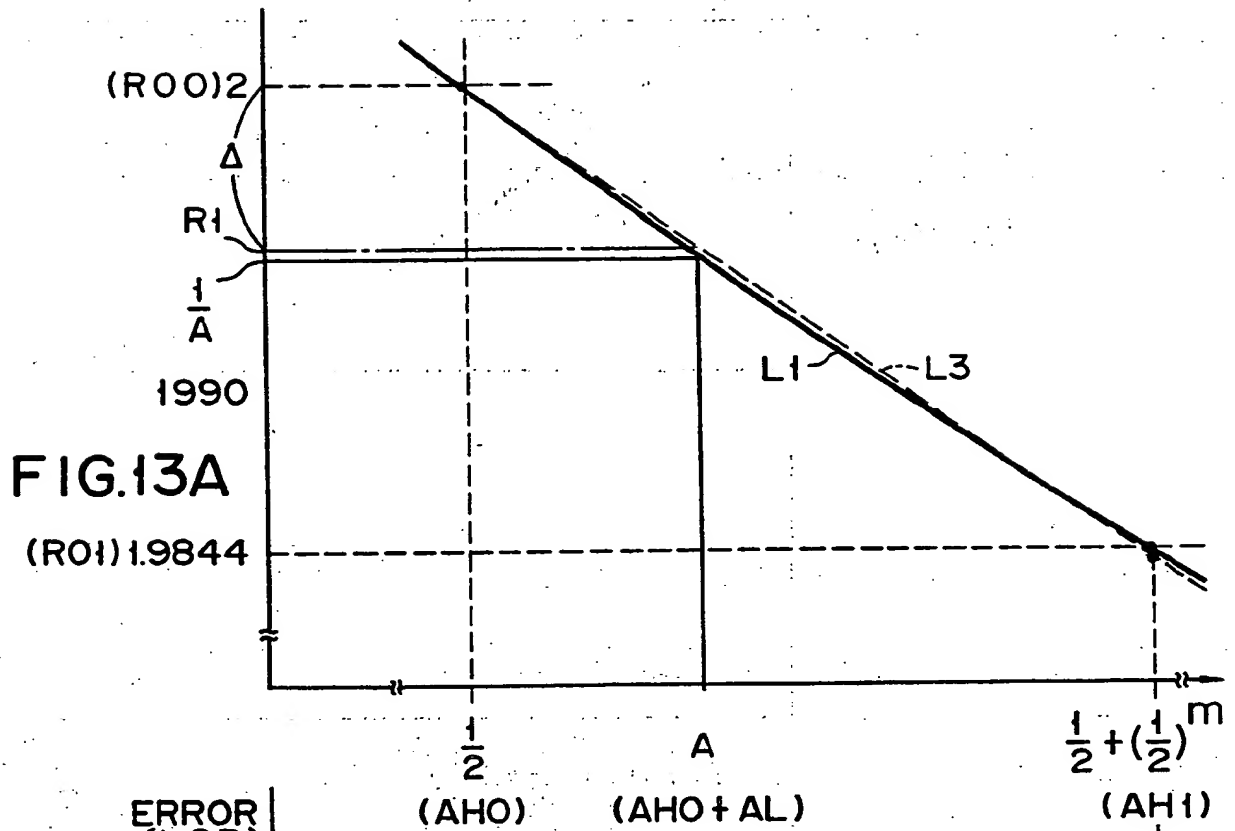


FIG.12B





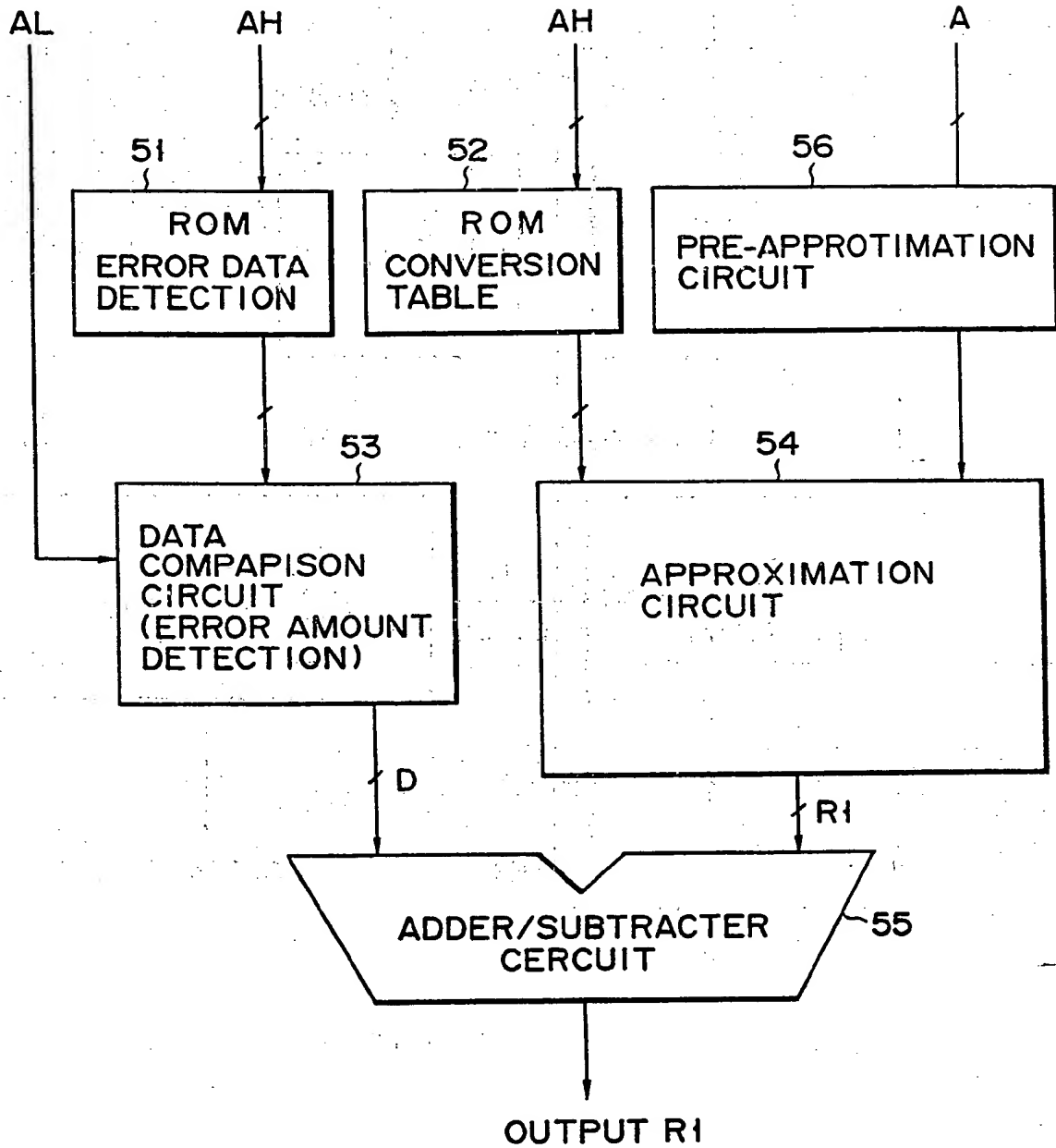


FIG. 14



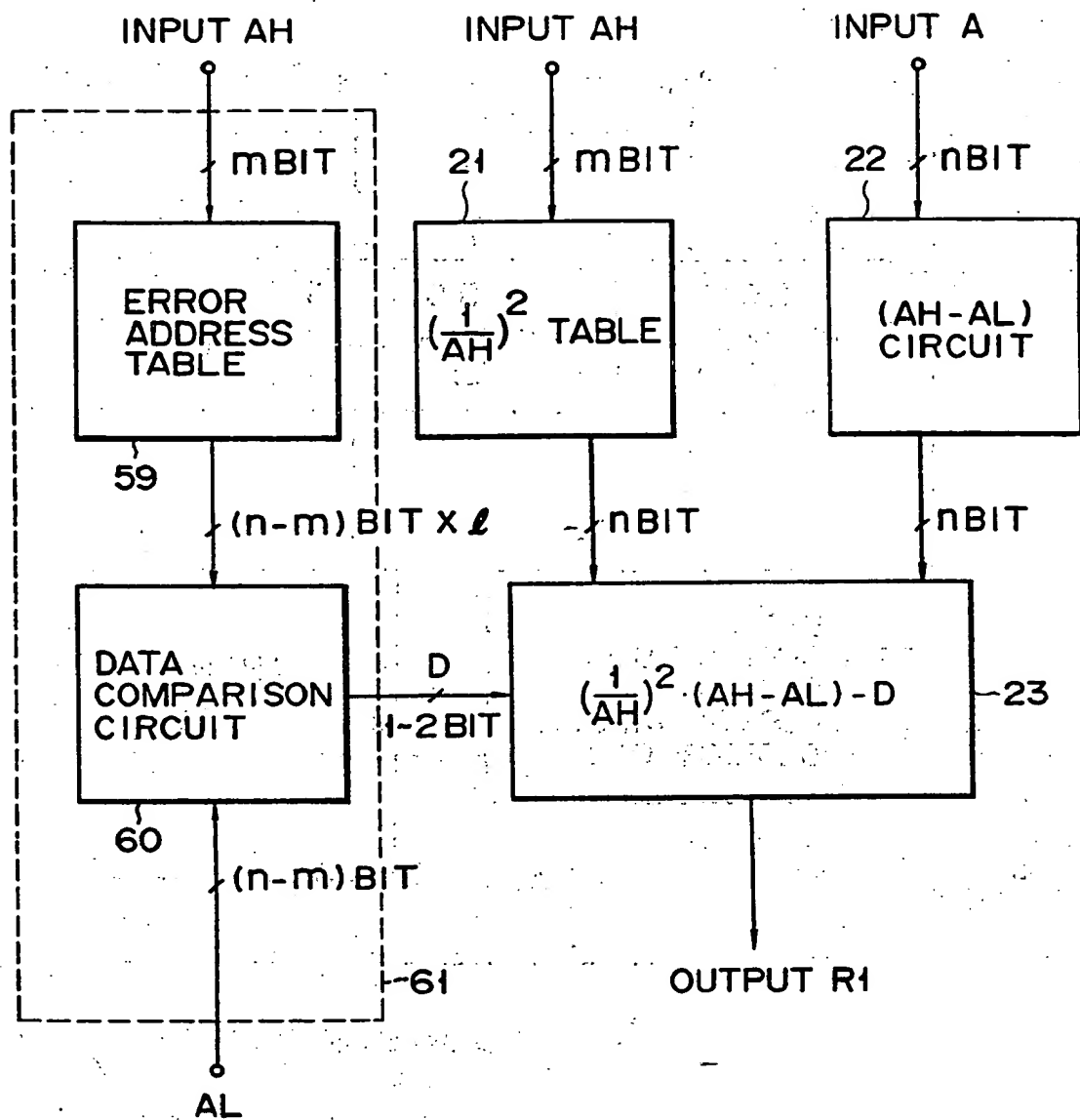


FIG. 15

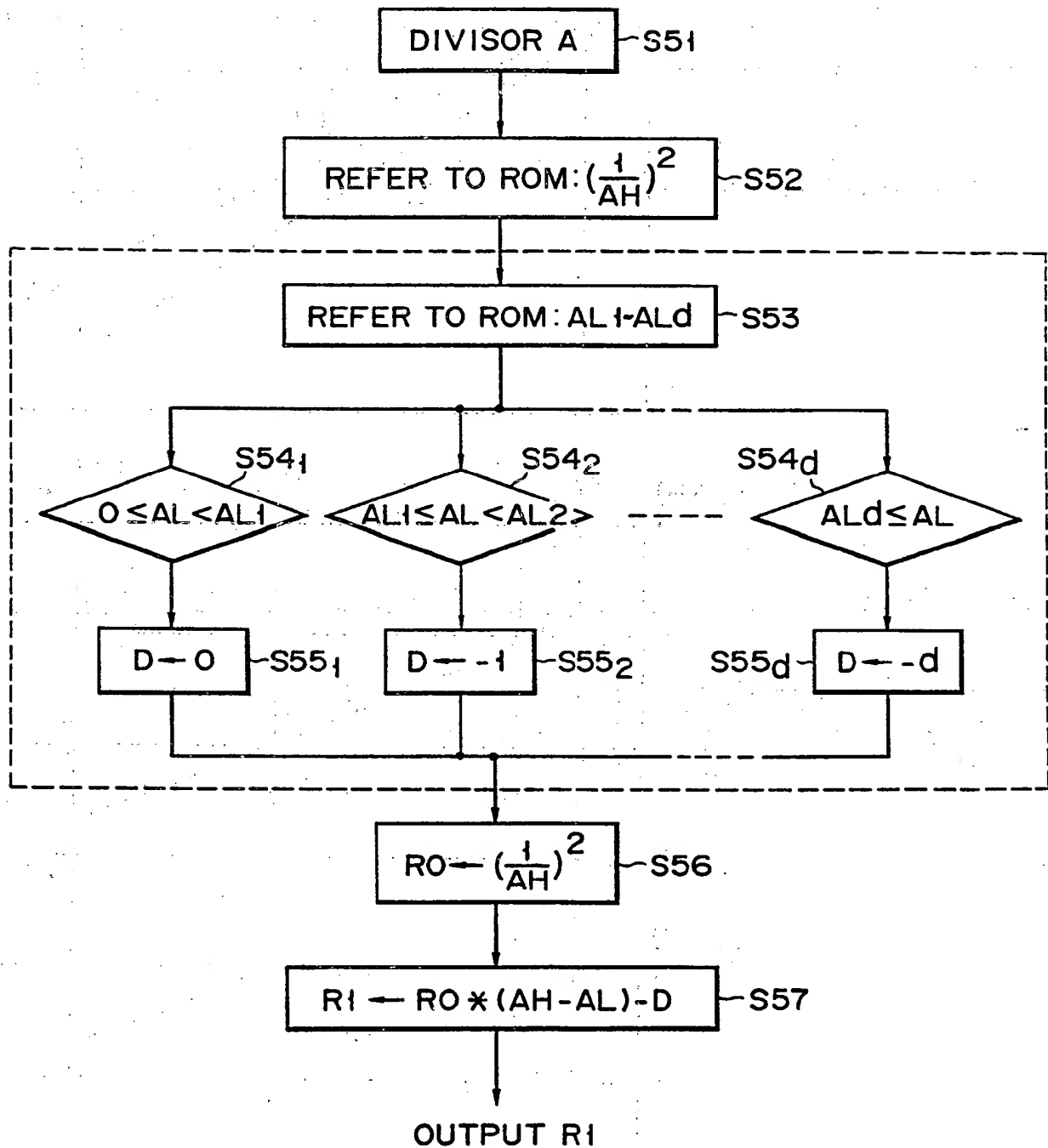


FIG. 16

FIG. 17A

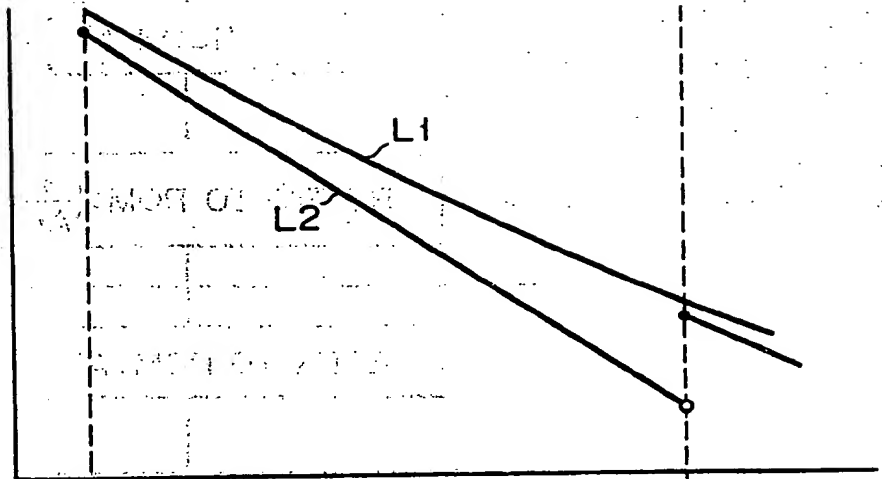


FIG. 17B

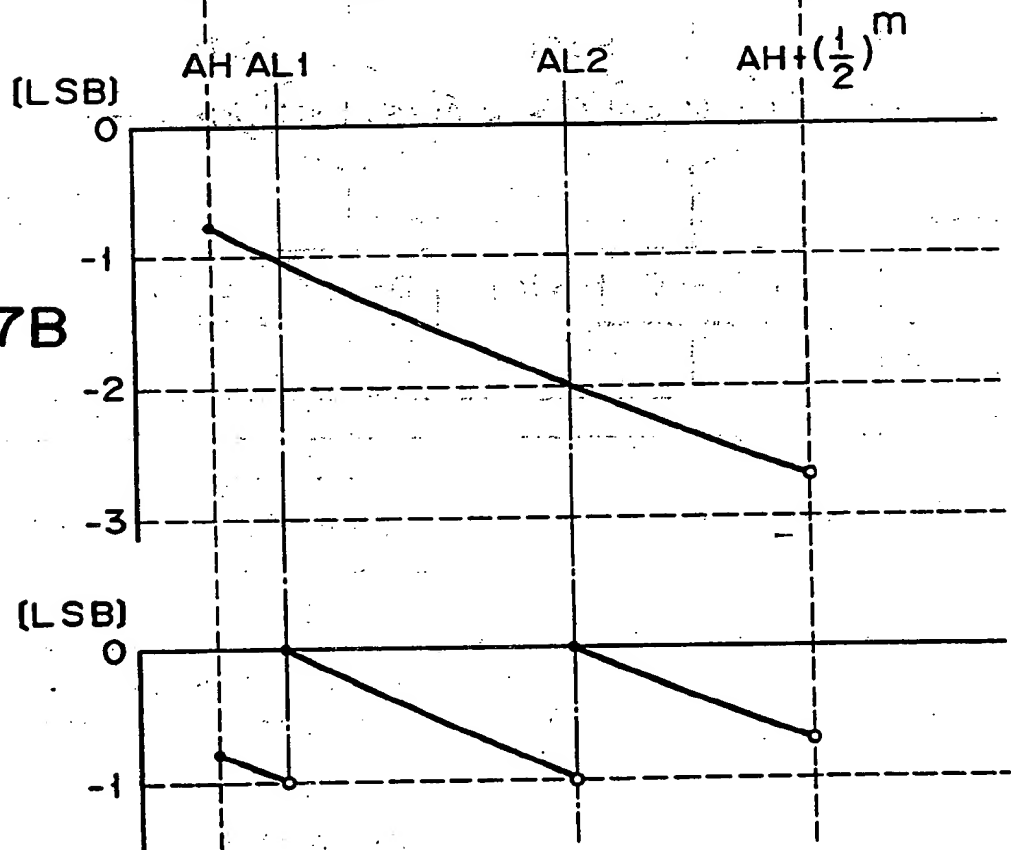


FIG. 17C

FIG. 18A

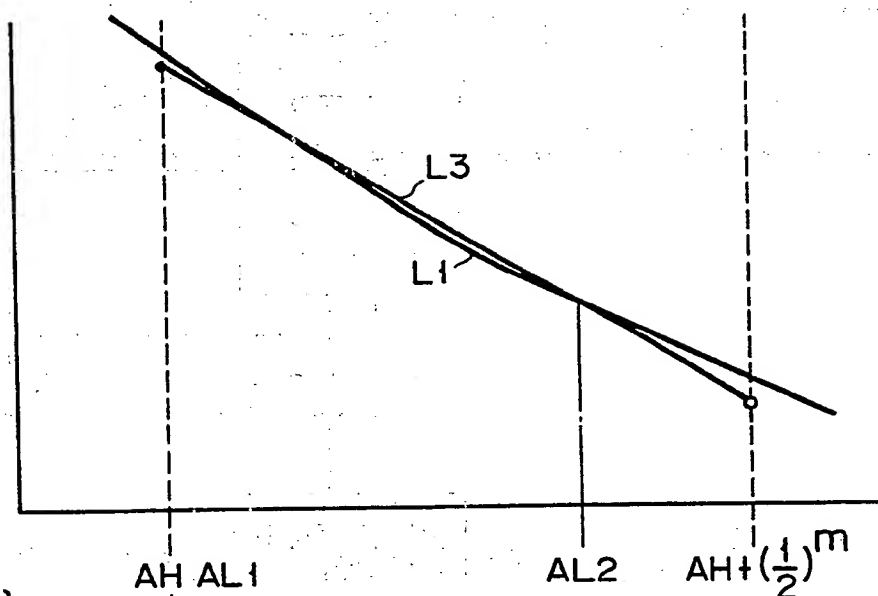


FIG. 18B

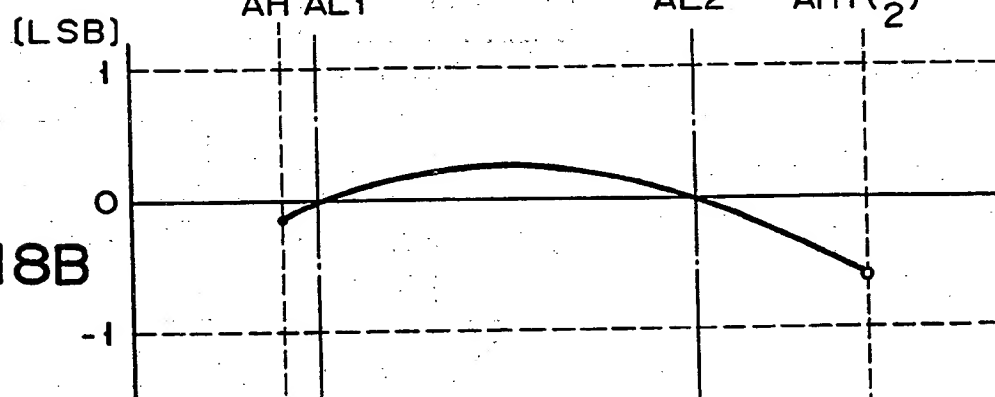
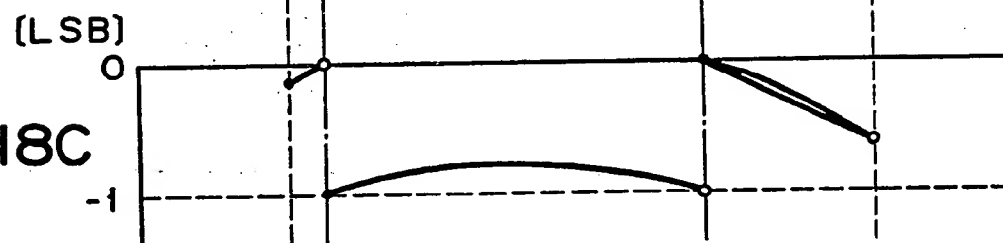


FIG. 18C



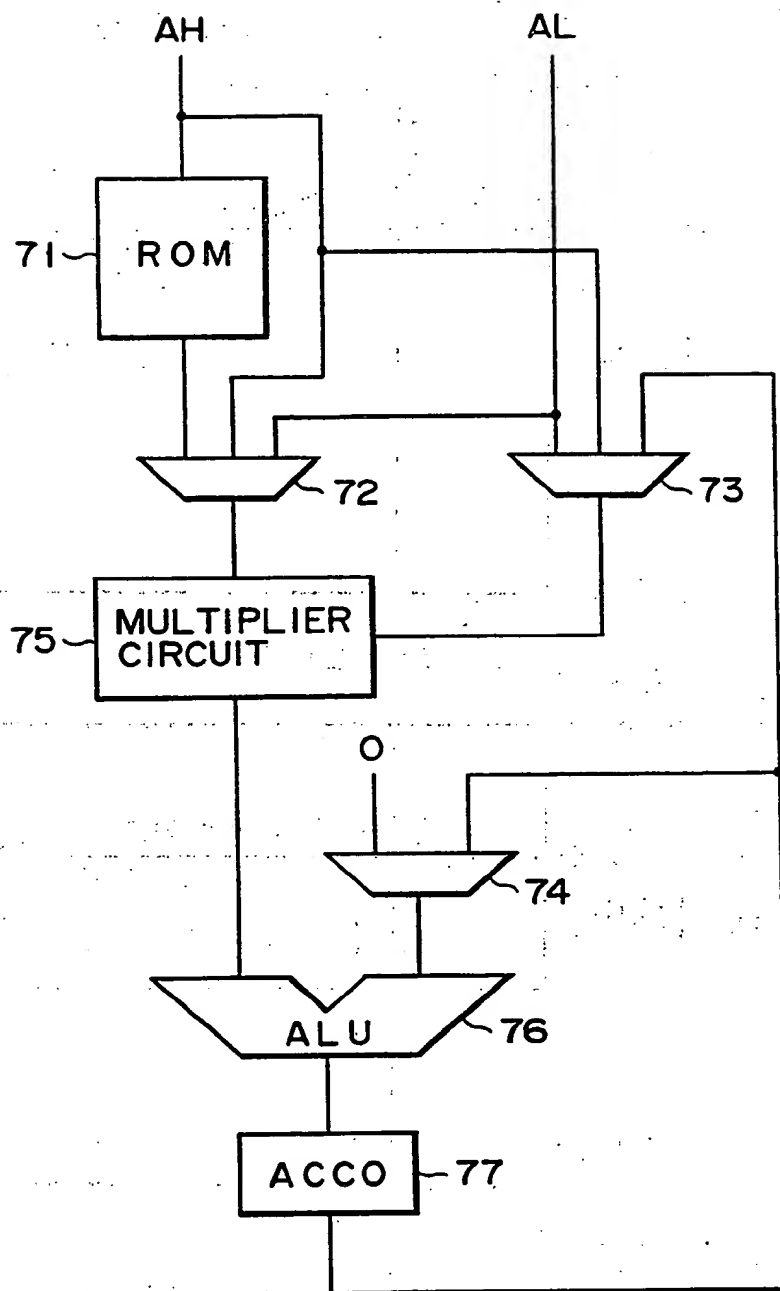


FIG. 19

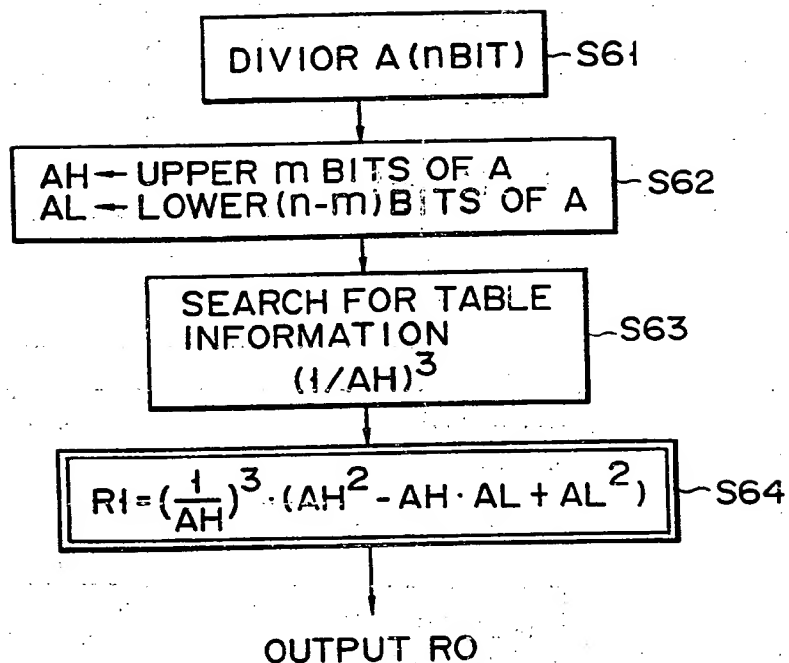


FIG. 20

| n  | CONVENTIONAL CIRCUIT (m) |                 | (m) THIS INVENTION |
|----|--------------------------|-----------------|--------------------|
|    | FULL-BIT SYSTEM          | NEWTON'S METHOD |                    |
| 8  | 8                        | 4               | 3                  |
| 16 | 16                       | 8               | 6                  |
| 24 | 24                       | 12              | 8                  |
| 32 | 32                       | 16              | 11                 |

FIG. 21

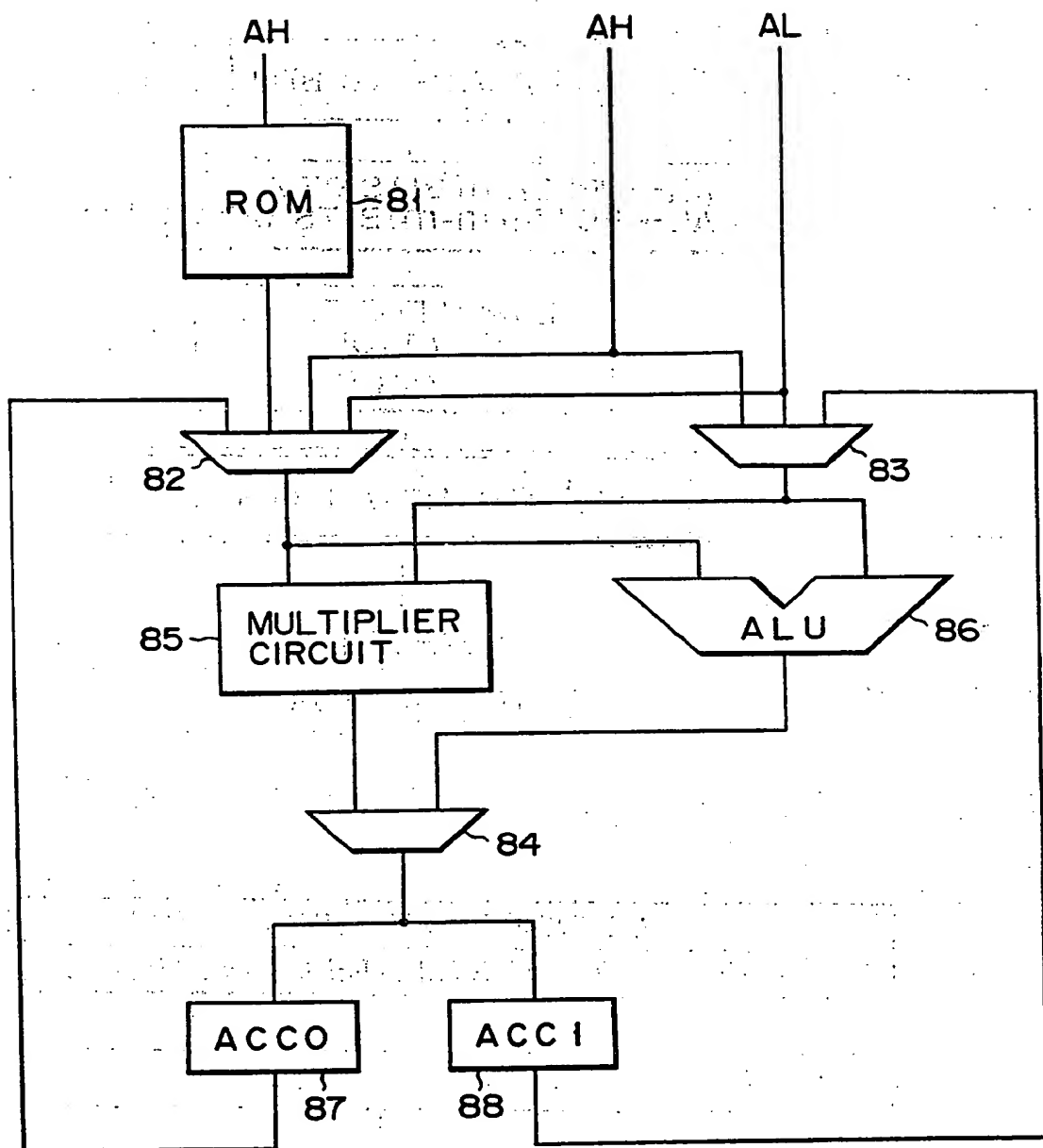


FIG. 22

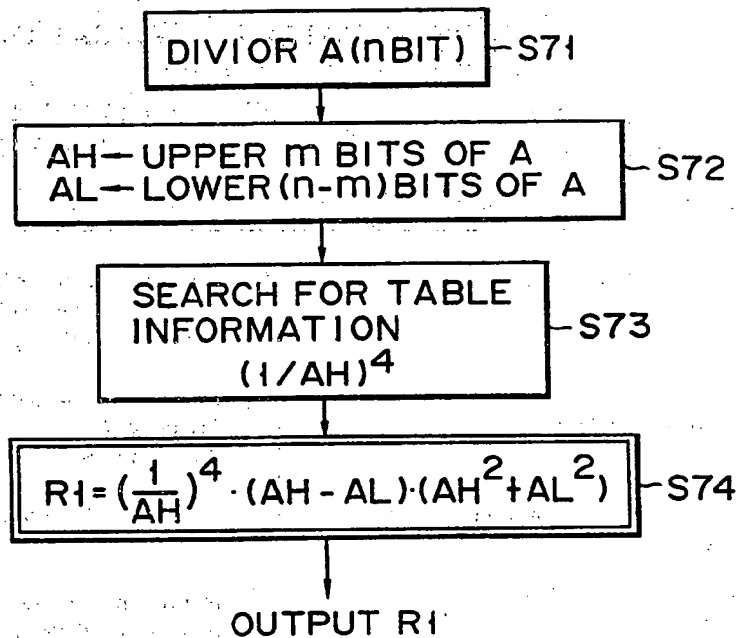


FIG. 23

| n  | CONVENTIONAL CIRCUIT (m) |                | (m) THIS INVENTION |
|----|--------------------------|----------------|--------------------|
|    | FULL - BIT SYSTEM        | NEWTONS METHOD |                    |
| 8  | 8                        | 4              | 2                  |
| 16 | 16                       | 8              | 4                  |
| 24 | 24                       | 12             | 6                  |
| 32 | 32                       | 16             | 8                  |

FIG. 24





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Publication number:

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12

## EUROPEAN PATENT APPLICATION

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### 54 Reciprocal arithmetic circuit with ROM table.

57 A reciprocal arithmetic circuit for deriving the reciprocal of a divisor A includes a ROM table (21) for converting upper-bit data AH supplied as an address to the approximation of the reciprocal  $1/AH^2$  of the square thereof and outputting the same; a subtracter circuit (22) for deriving a difference (AH-AL) between the upper-bit data AH and the lower-bit data AL of the divisor A, and a multiplier circuit (23) for receiving an output  $(1/AH^2)$  of the ROM table (21) and an output (AH-AL) of the subtracter circuit and deriving the product  $(1/AH^2) \times (AH-AL)$  thereof to make the output  $(1/AH^2)$  of the ROM table more nearly equal to the reciprocal  $1/A$  of the divisor A.

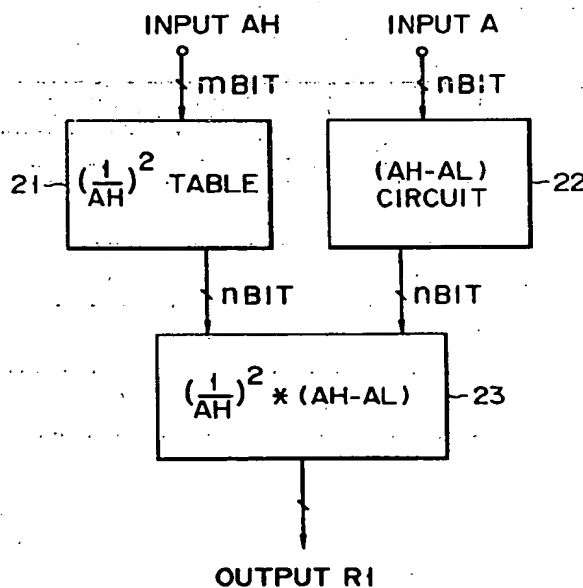


FIG. 4

EP 0 372 566 A3



European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number

EP 89 12 2680

| DOCUMENTS CONSIDERED TO BE RELEVANT  |   |  |   |
|--|---|--|---|
| Category   | Citation of document with indication, where appropriate, of relevant passages   | Relevant to claim  | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
| A  | EP-A-0 149 248 (HITACHI)<br>* abstract; claim 7; figure 14 *  | 1, 10, 11  | G06F1/035<br>G06F7/52<br>G06F101/12           |
| A  | * page 5, line 6 - page 6, line 4 *   | 4-9  |   |
| A  | GB-A-2 204 433 (SUN MICROSYSTEMS INC)<br>* abstract; claims 1,5; figure 2 *   | 1, 4   |   |
| A  | ALTA FREQUENZA<br>vol. 48, no. 11, November 1979, MILANO, IT<br>pages 690 - 693;<br>R. STEFANELLI: 'Binary read-only-memory dividers'<br>* the whole document * | 1, 4   |   |
|  |   |  | TECHNICAL FIELDS SEARCHED (Int. Cl.5)         |
|  |   |  | G06F  |
| The present search report has been drawn up for all claims   |   |  |   |
| Place of search<br>THE HAGUE   |   | Date of completion of the search<br>14 SEPTEMBER 1992  | Examiner<br>COHEN B.                          |
| <b>CATEGORY OF CITED DOCUMENTS</b>   |   |  |   |
| X : particularly relevant if taken alone<br>Y : particularly relevant if combined with another document of the same category<br>A : technological background.<br>O : non-written disclosure<br>P : intermediate document |   | T : theory or principle underlying the invention<br>E : earlier patent document, but published on, or after the filing date<br>D : document cited in the application<br>L : document cited for other reasons<br>& : member of the same patent family, corresponding document |   |



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### CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

### LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

See Sheet B.

- ☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:
- ☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:



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EP 89 12 2680-B-

### LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-3,10,11: Reduction of division hardware complexing by using a first approximation of  $1/AH_n$  from ROM ( $n7,2$ )
2. Claims 4-9: Reduction of division hardware complexity by using a first approximation of  $1/AH$  and  $1/AH+1/2m$  from ROM.